

8	7
THIS DRAWING AND SPECIFICATIONS, HEREIN, ARE THE PROPERTY OF INVENTEC CORPORATION AND SHALL NOT BE REPRODUCED, COPIED, OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION, INVENTEC CORPORATION, 2009 ALL RIGHT RESERVED.	

HSF Property:ROHS or Halogen-Free(5L3?)

GL10FH

2011.09.08

21-OCT-2002		
DATE	CHANGE NO.	REV

DRAWER		EE	DATE	POWER	DATE	<div style="text-align: center;"> <h1>INVENTEC</h1> </div>			
DESIGN									
CHECK									
RESPONSIBLE									
SIZE=					VER:	TITLE		MODEL,PROJECT,FUNCTION	
FILE NAME:						Everest Main Board			
P/N		XXX				SIZE C	CODE CS	DOC NUMBER	REV
							1310xxxxxx-0-0		X01
					SHEET		1 of 70		

TABLE OF CONTENTS

PAGE

- 1. COVER PAGE
- 2. INDEX
- 3. BLOCK DIAGRAM
- 4. POWER MAP
- 5. POWER CHARGER
- 6. POWER +V3LA/+V3A/+5A
- 7. POWER +V1.5/+V0.75
- 8. POWER +V1.8S
- 9. POWER VCCIO
- 10. POWER VCCSA
- 11. POWER VCORE
- 12. POWER VGFX
- 13. POWER VCORE_DGPU
- 14. ENABLE PIN
- 15. LOAD SWITCH-1
- 16. LOAD SWITCH-2(FOR OPTIMUS)
- 17. PCB SCREW
- 18. HALL SENSOR
- 19. LED
- 20. K/B & TP/B CONN
- 21. EC
- 22. LAN
- 23. RJ45 & TRANSFORMER
- 24. AUDIO CODEC
- 25. SPEAKER/HP JACK/MIC JACK

PAGE

- 26. AMP
- 27. CARDREADER
- 28. MINI1 WLAN/DEBUG CARD
- 29. MINI2 3G/LTE
- 30. B-CAS
- 31. SATA HDD/ODD CONN
- 32. USB 2.0 CONN
- 33. USB 3.0 CONTROLLER
- 34. USB 3.0 CONN W/ S&C
- 35. USB 3.0 CONN
- 36. EDP CONN
- 37. LCM CONN
- 38. CRT CONN
- 39. HDMI CONN
- 40. HDMI CEC
- 41. DDR3 DIMM0
- 42. DDR3 DIMM1
- 43. DDR3 DIMM0
- 44. DDR3 DIMM1
- 45. FAN & THERMAL SENSOR
- 46. CPU 1
- 47. CPU 2
- 48. CPU 3 DRAM
- 49. CPU 4 POWER
- 50. CPU 5 POWER

PAGE

- 51. CPU 6 GND
- 52. PCH 1
- 53. PCH 2
- 54. PCH 3
- 55. PCH 4 AXG
- 56. PCH 5 USB
- 57. PCH 6 MISC
- 58. PCH 7 POWER
- 59. PCH 8 POWER
- 60. PCH 9 GND
- 61. MXM CONNECTOR 1
- 62. MXM CONNECTOR 2
- 63. POWER BUTTON BOARD
- 64. EMI
- 65. 3D SENSOR
- 66. CIR
- 67. USB REDRIVER
- 68. CIR
- 69. LOGO LED
- 70. ECO BUTTOM

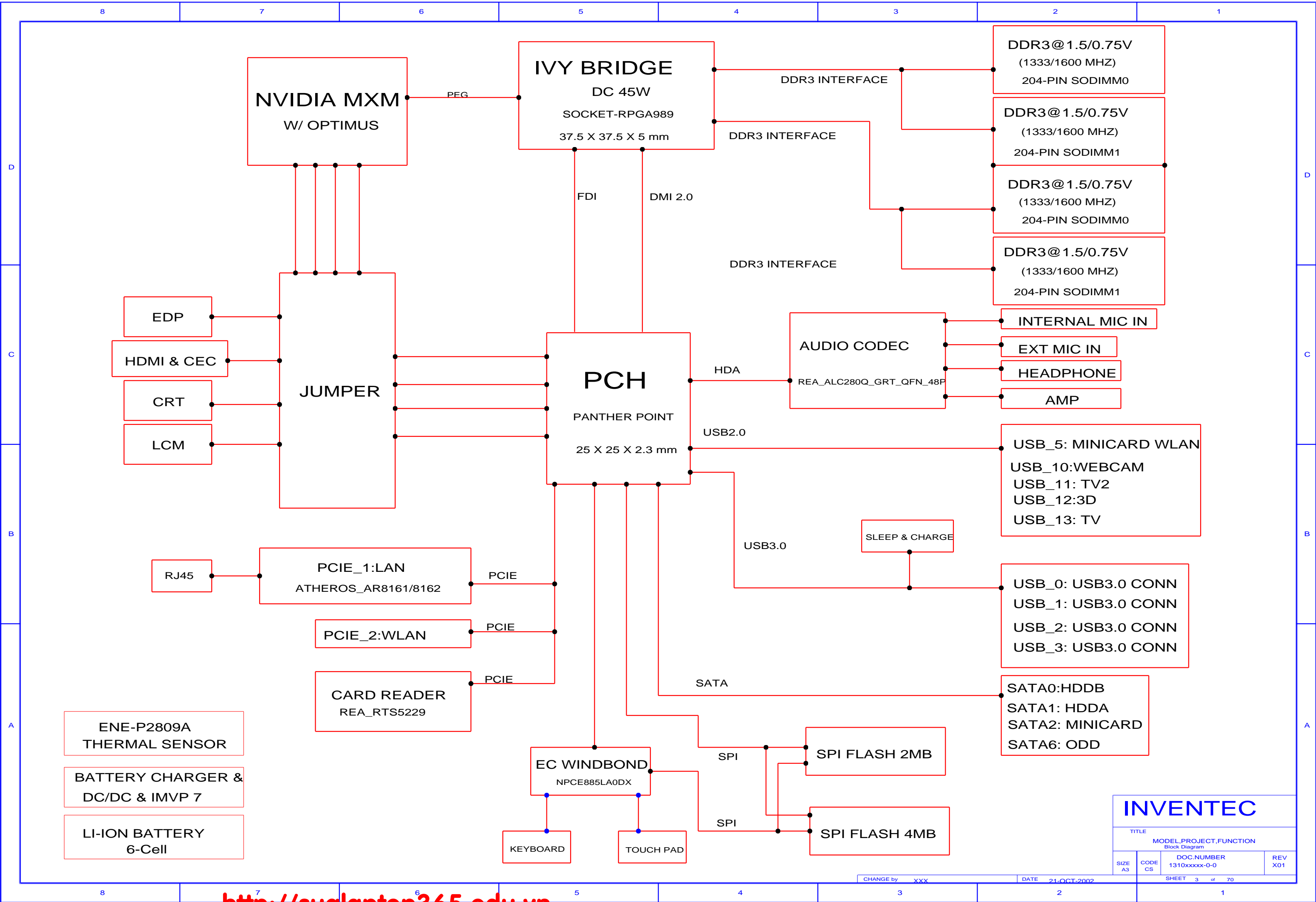
INVENTEC

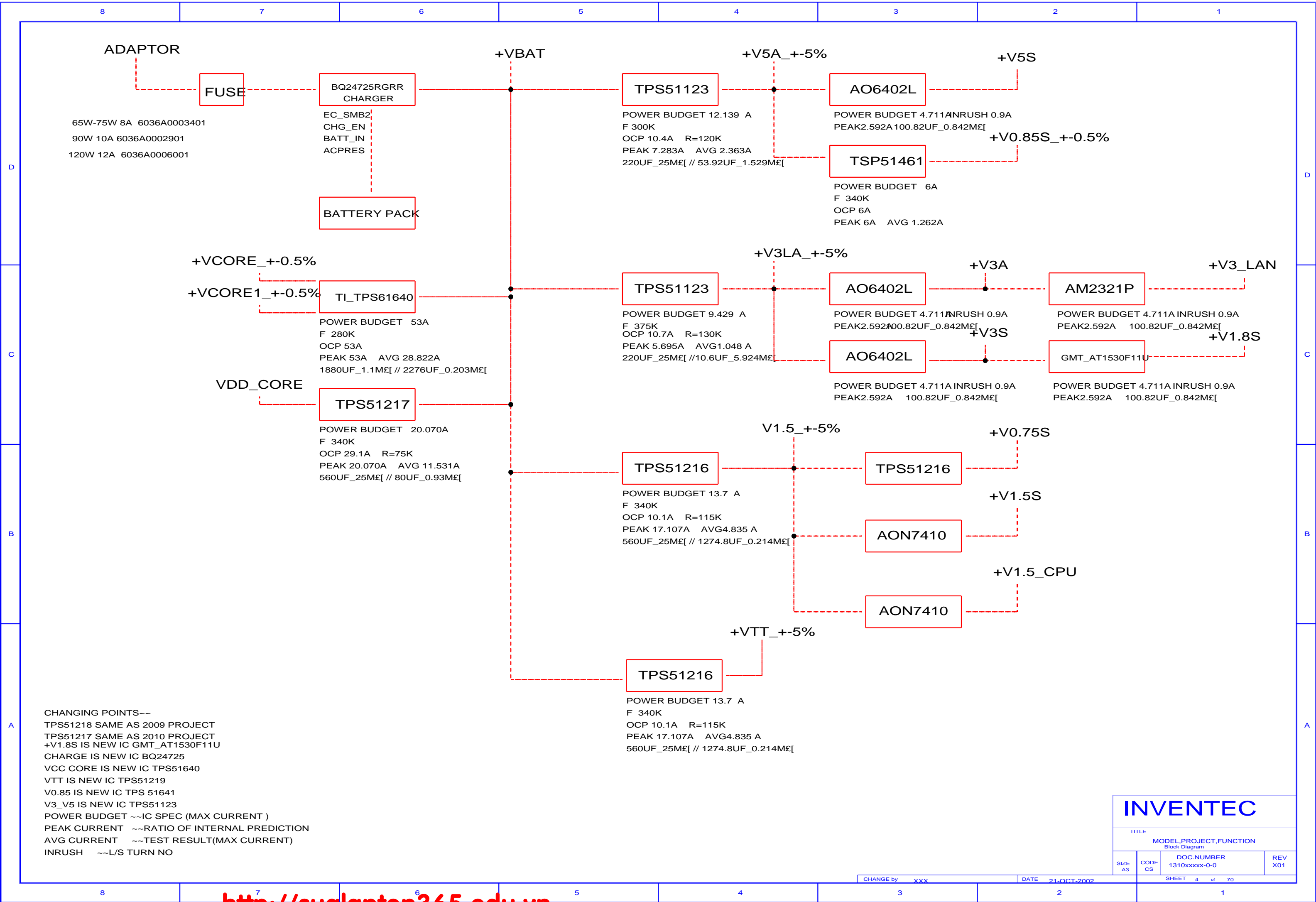
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
------------	------------	----------------------------	------------

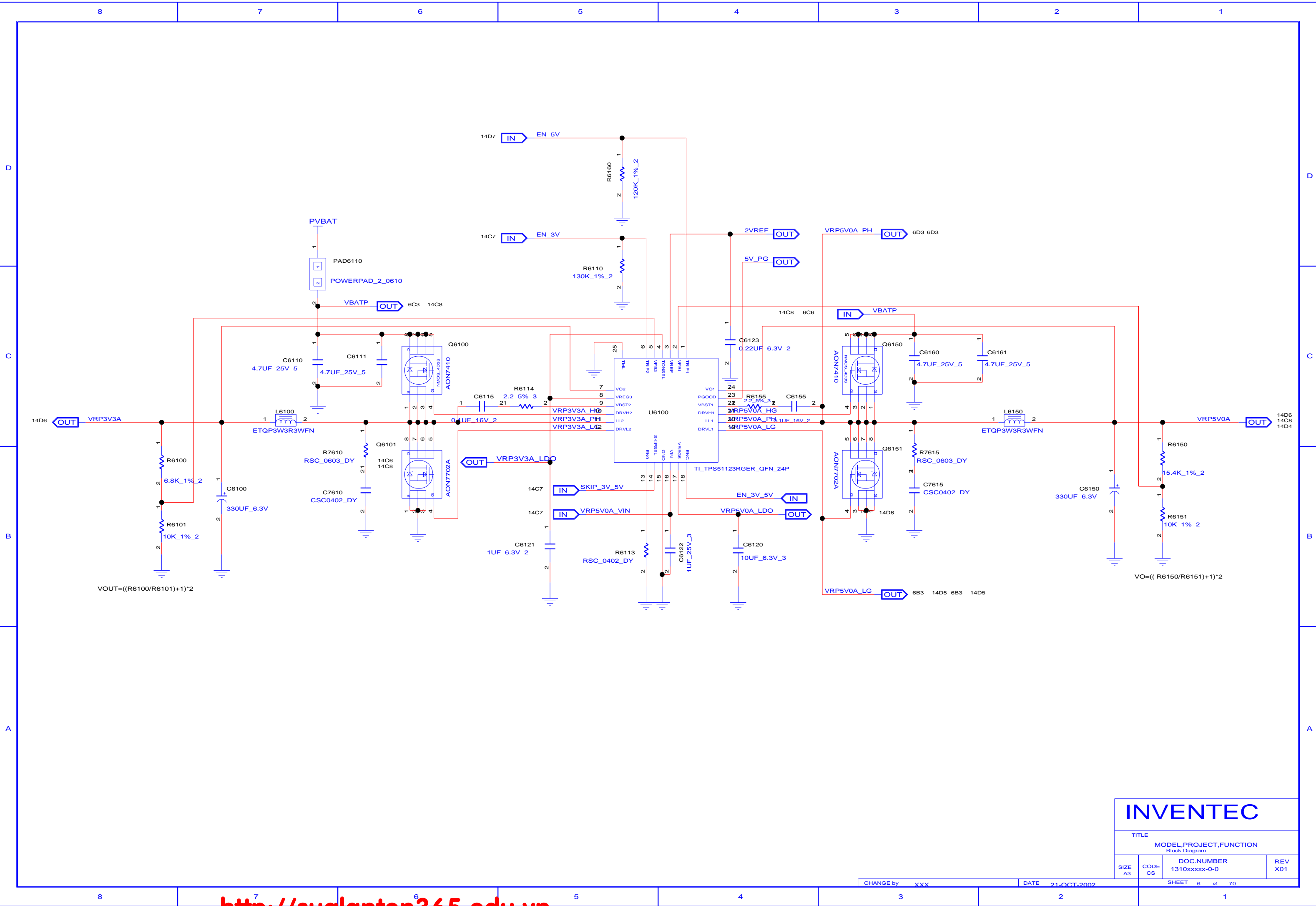
CHANGE by XXX DATE 21-OCT-2002

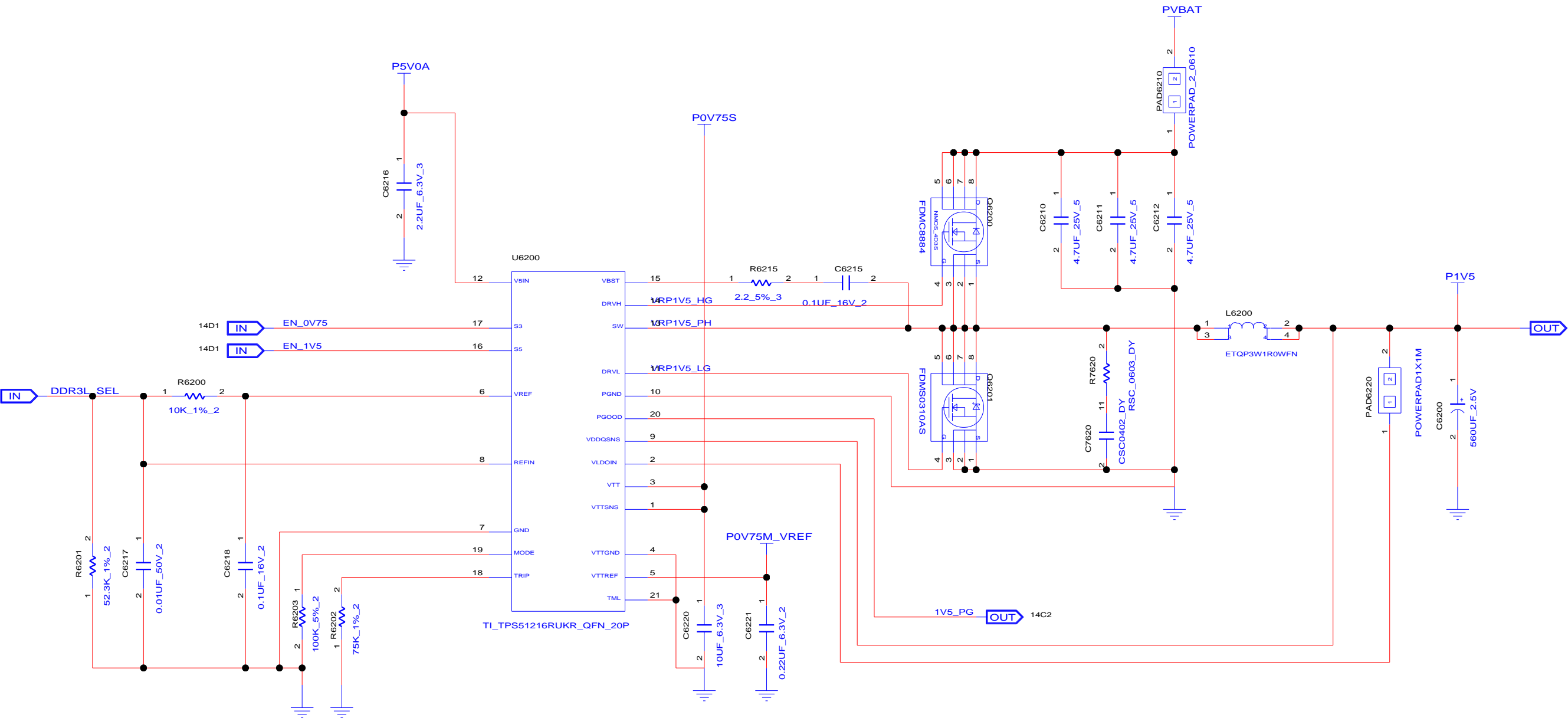
SHEET 2 of 70









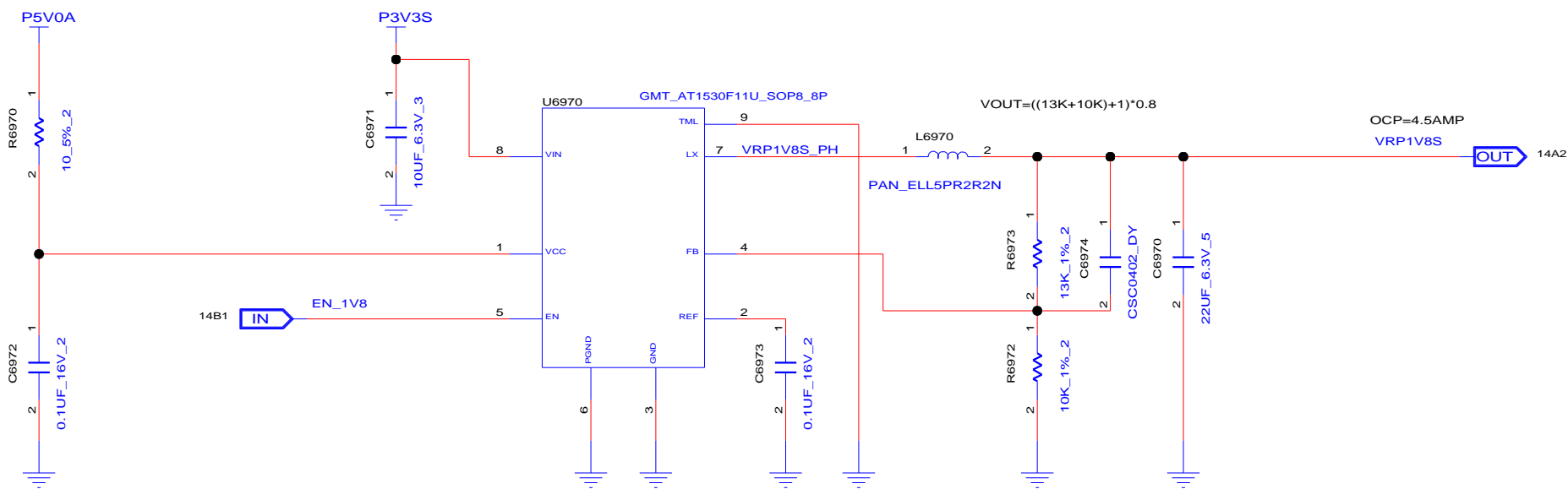


$$V_{OUT}=V_{REFIN}=1.8 \times \frac{R_{6201}}{R_{6200}+R_{6201}}$$

MODE=100KOHM:TRACKING DISCHARGE

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01



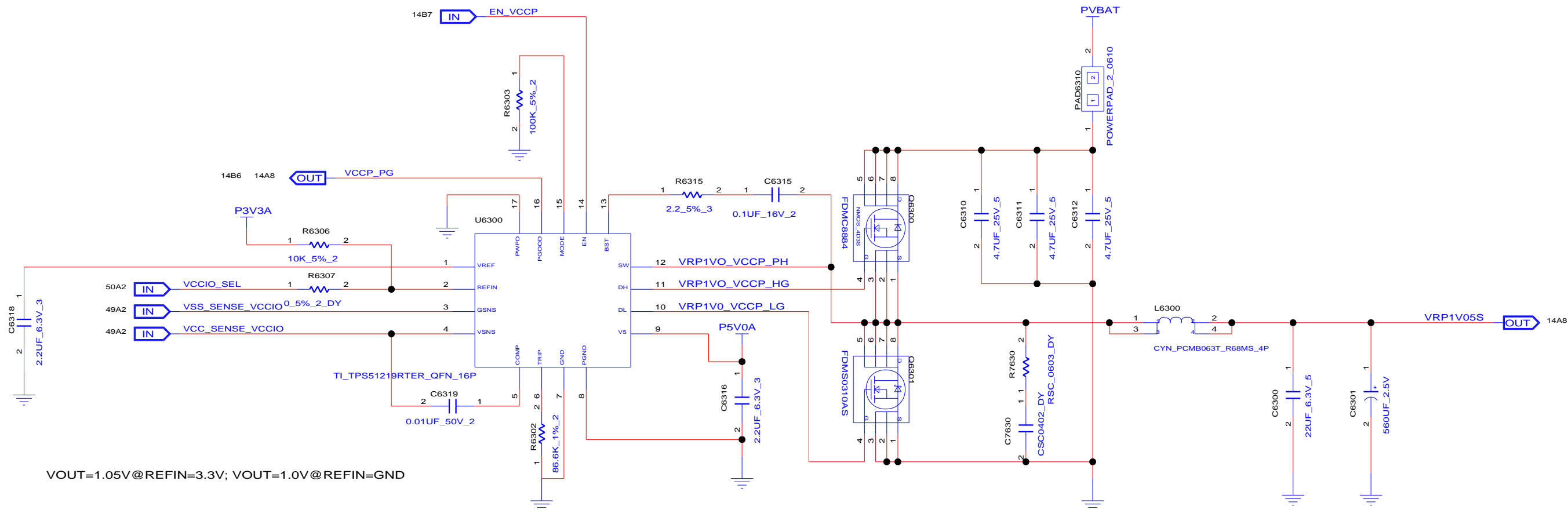
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

CHANGE by XXX DATE 21-OCT-2002

SHEET 8 of 70



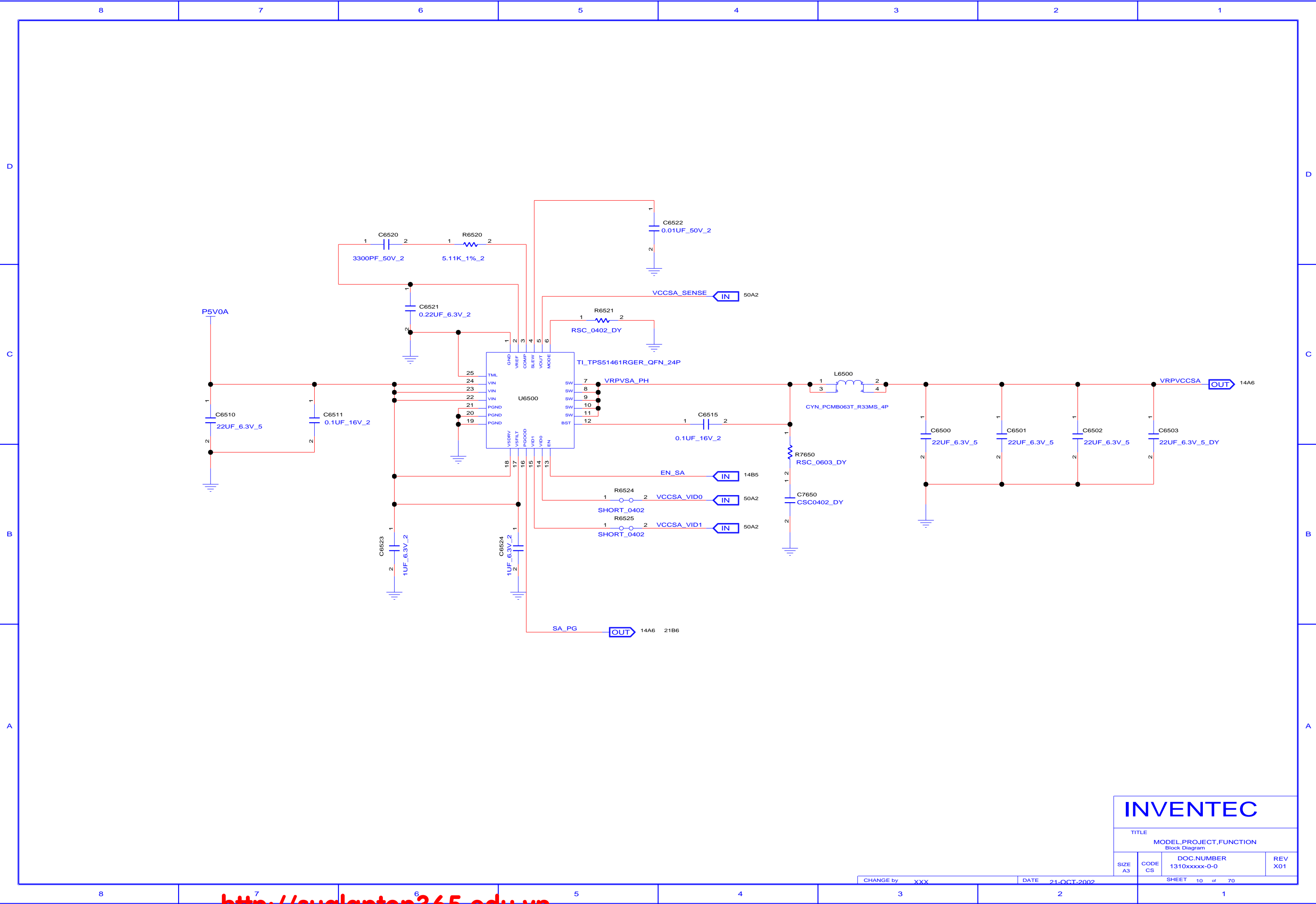
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC.NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 9 of 70





	8	7	6	5	4	3	2	1	
D									D
C									C
B									B
A									A
	8	7	6	5	4	3	2	1	

INVENTEC

TITLEMODEL,PROJECT,FUNCTIONBlock Diagram

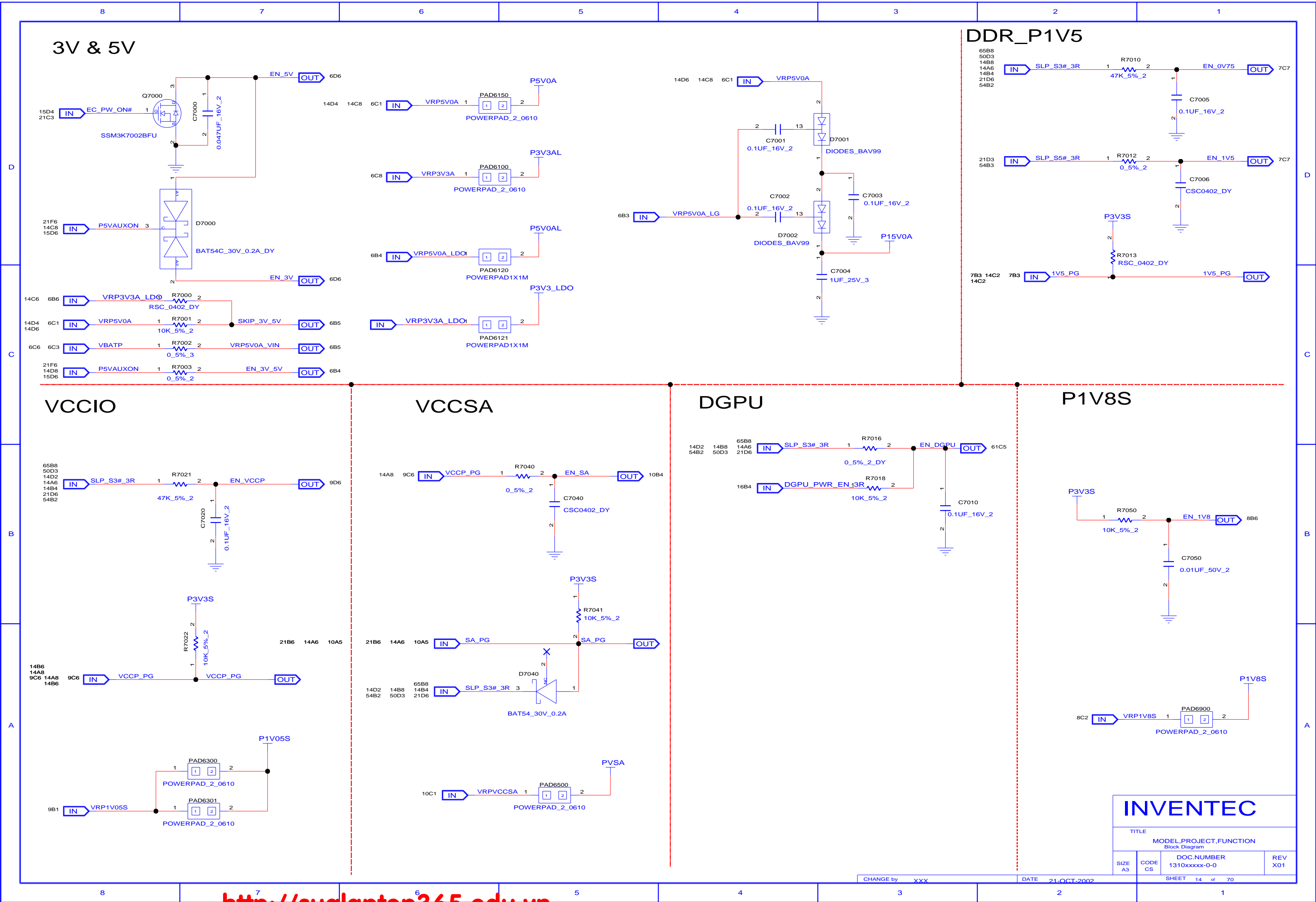
SIZEA3

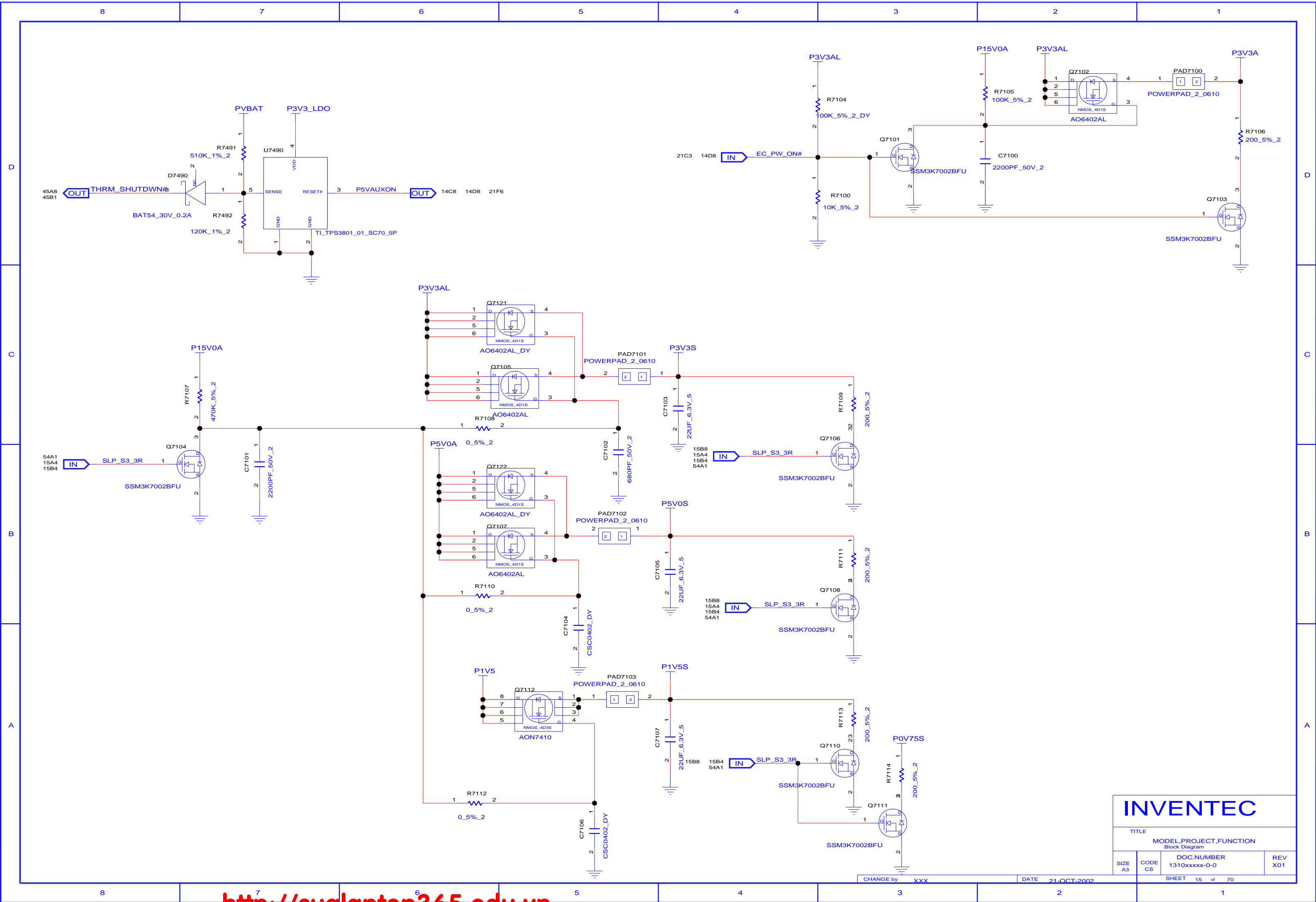
CODECS

DOC.NUMBER1310xxxxx-0-0

REVX01

CHANGE byXXXDATE21-OCT-2002SHEET13 of 70

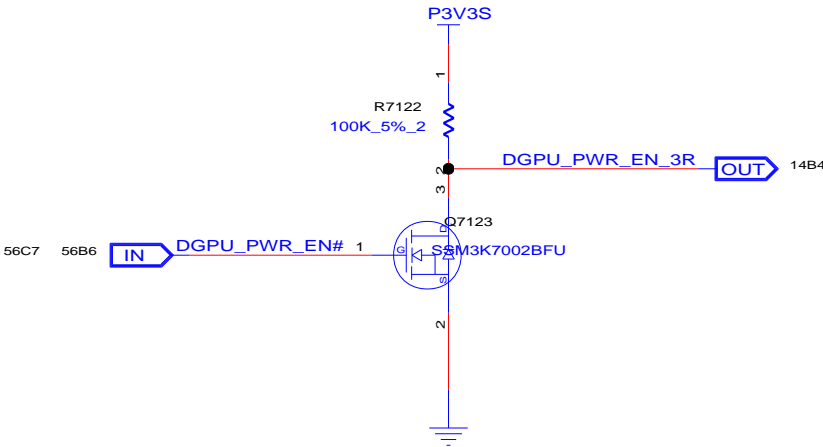


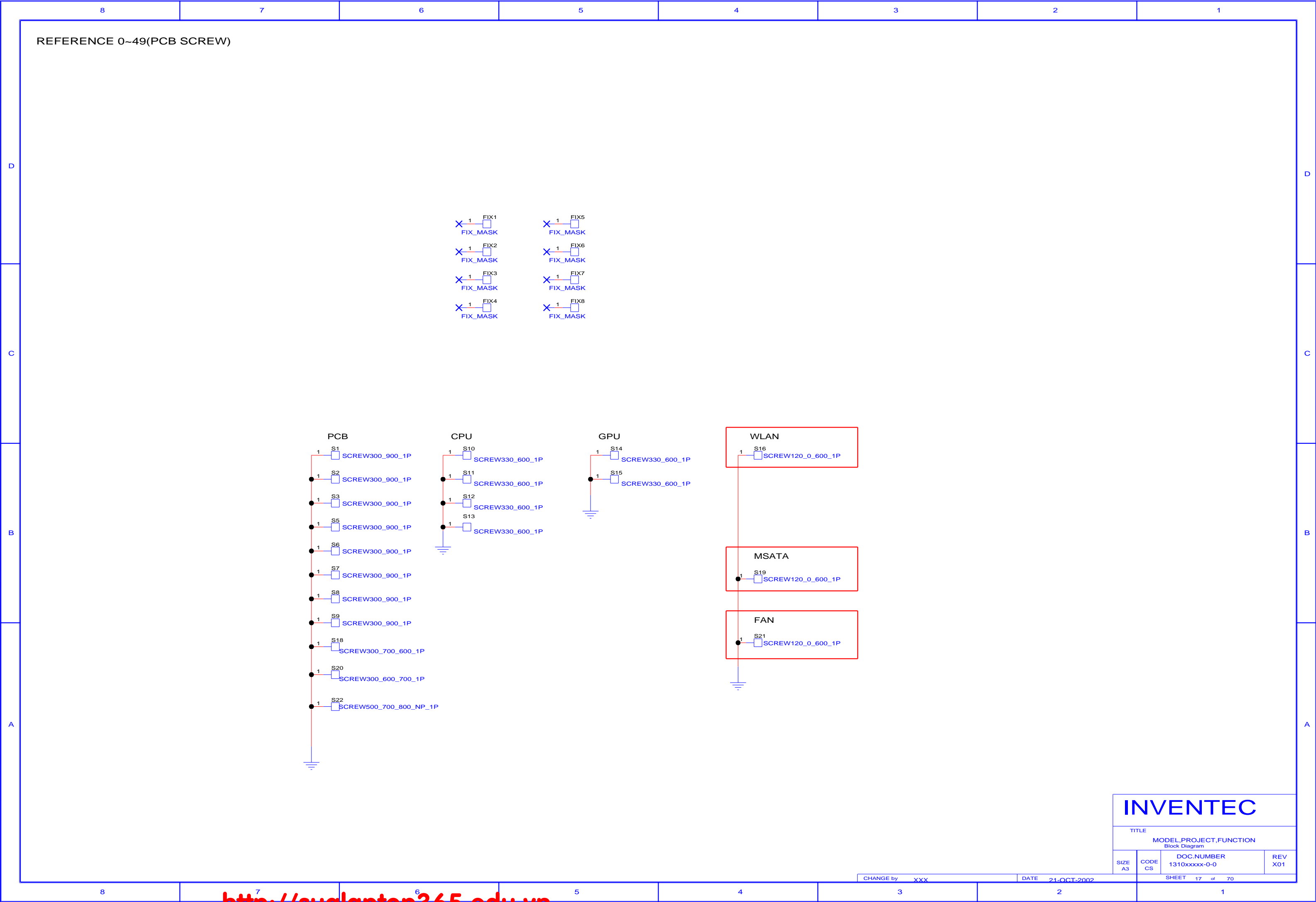


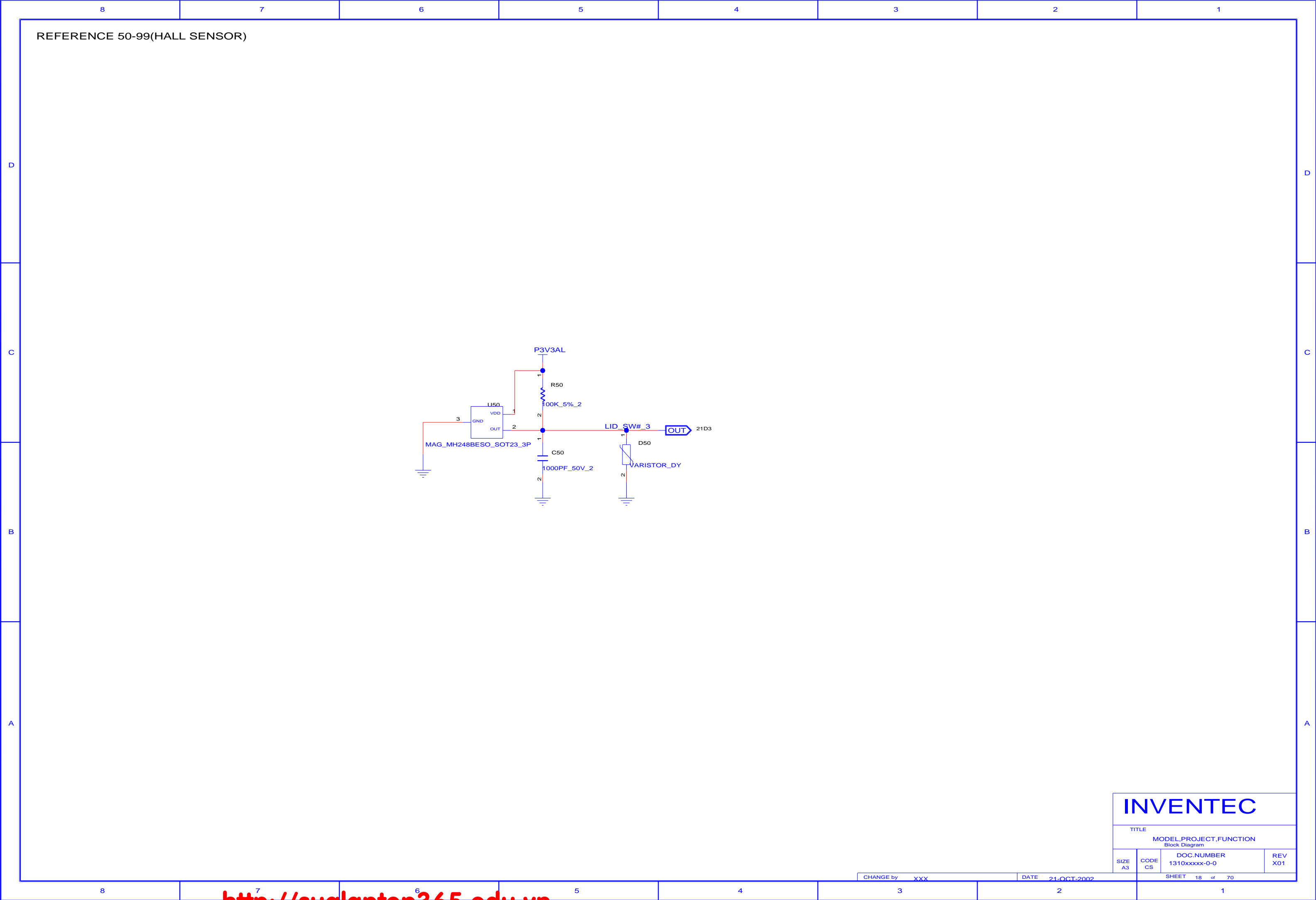
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 15 of 70

NVIDIA OPTIMUS

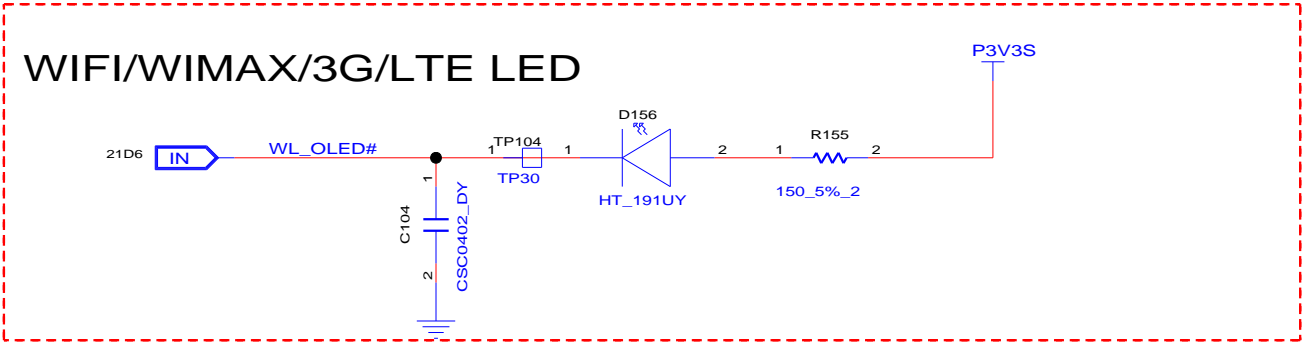
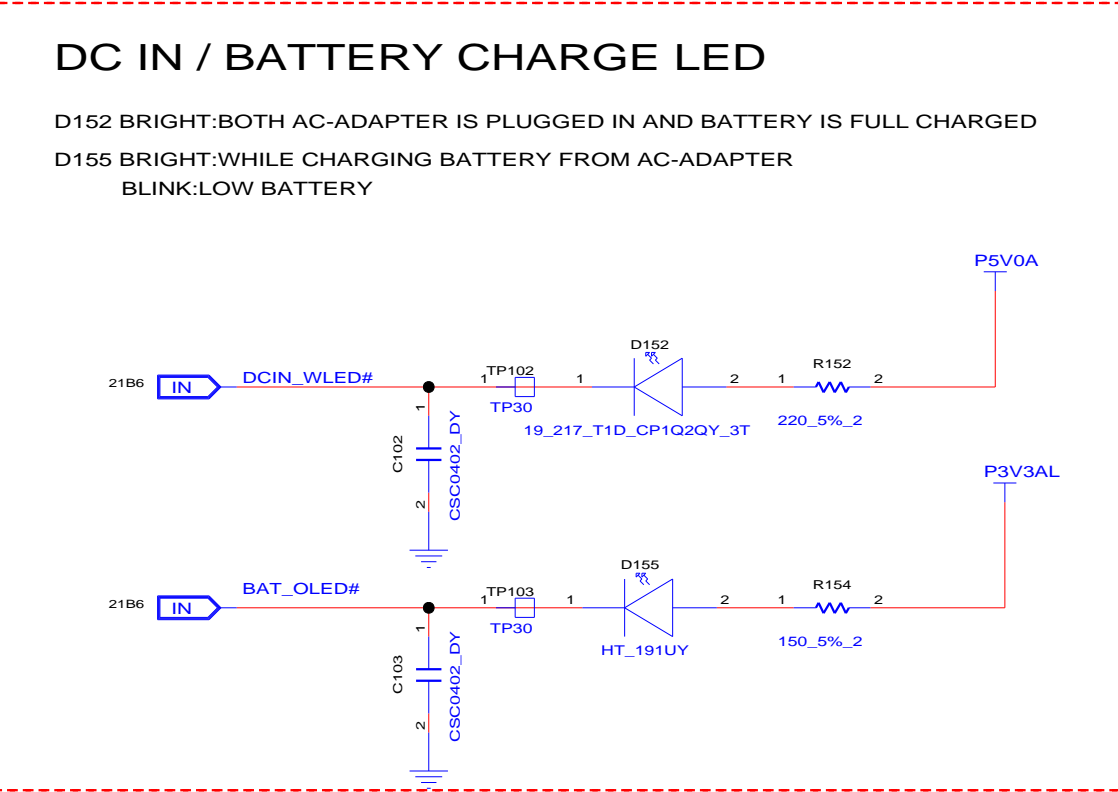
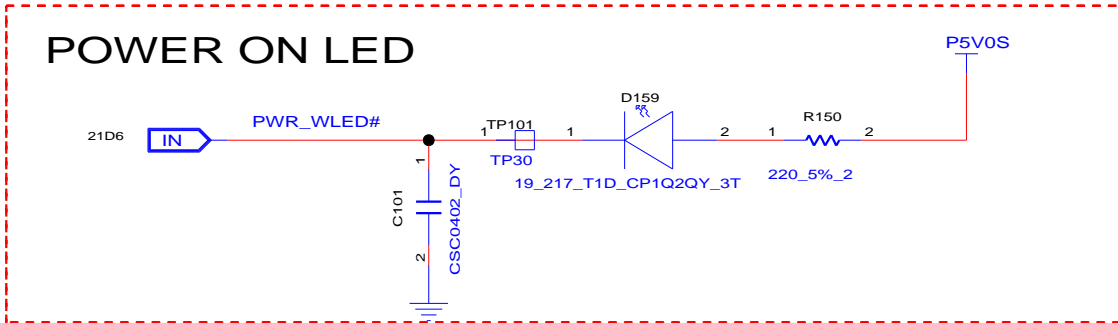
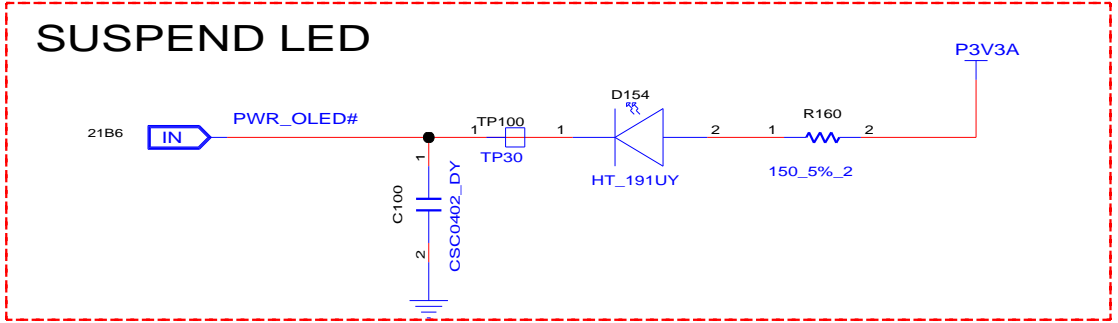
	DURING RESET	AFTER RESET	
DGPU_PWR_EN#	HIGH	HIGH	0 : DGPU POWER SWITCH TURNED ON 1 : POWER SWITCH TURNED OFF
DGPU_PG			0 : DGPU POWER IS NOT STABLE 1 : DGPU POWER IS STABLE
DGPU_HOLD_RST#	LOW	LOW	0 : KEEP DGPU IN RESET 1 : RESET IS RELEASED



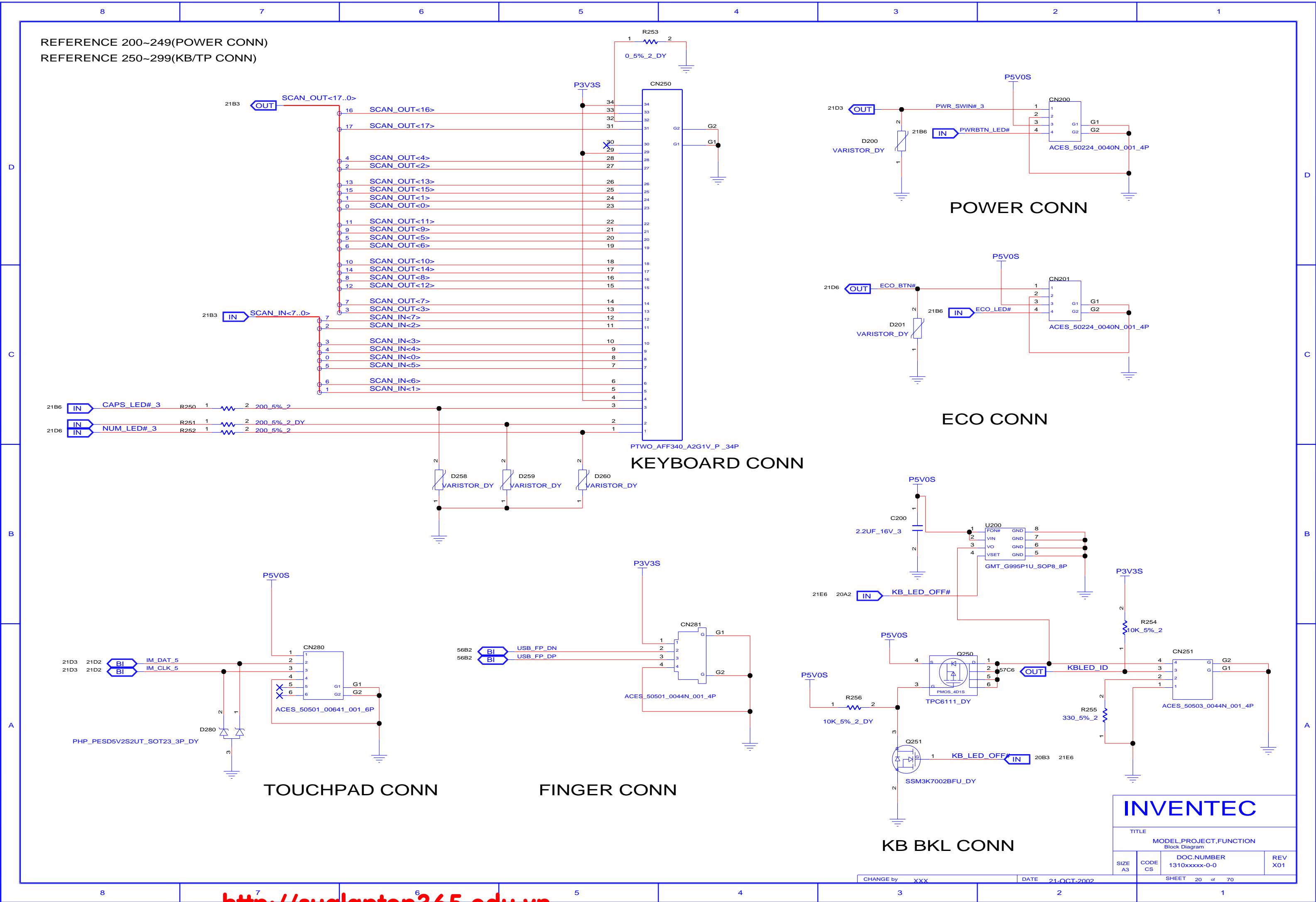




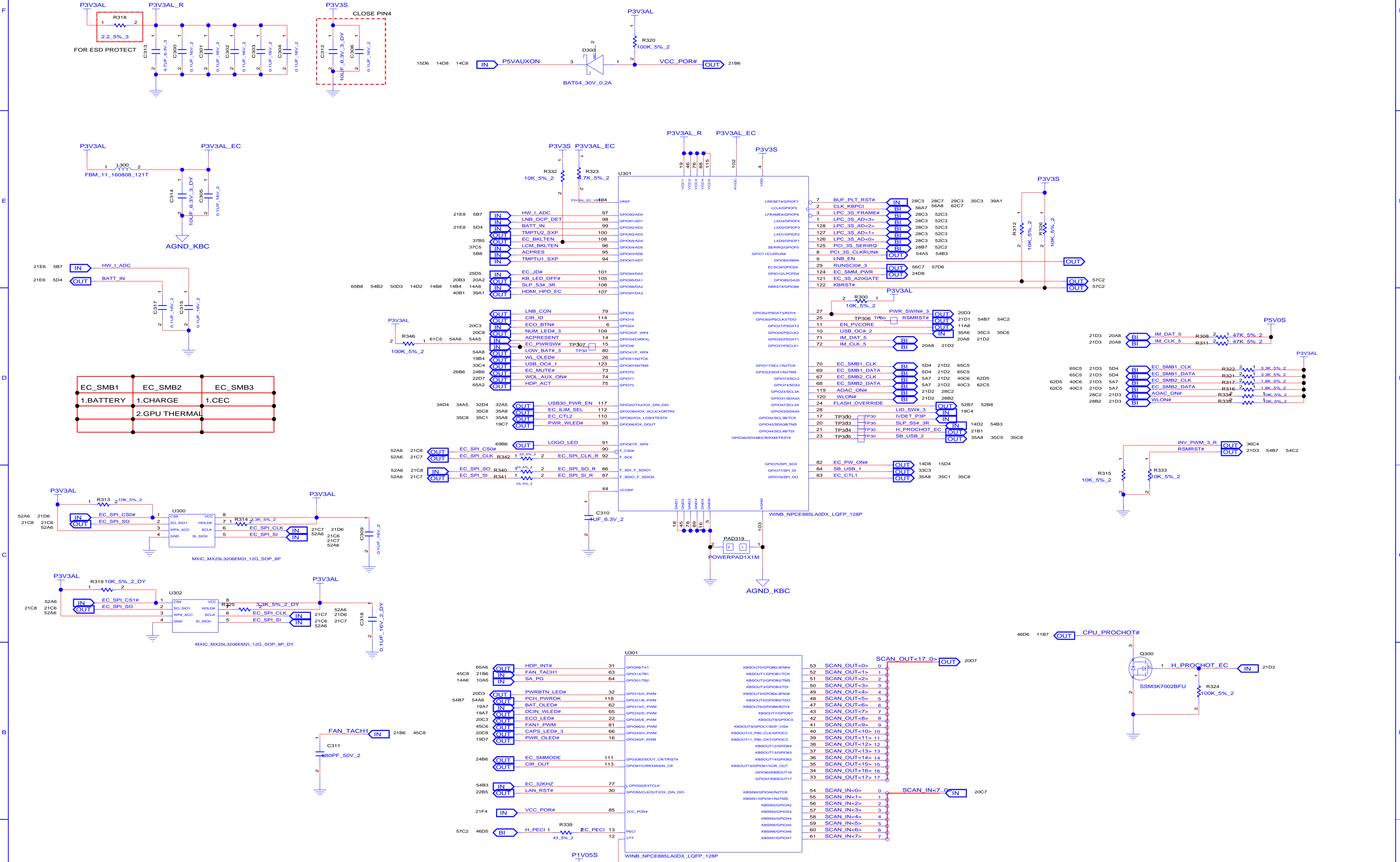
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 18 of 70

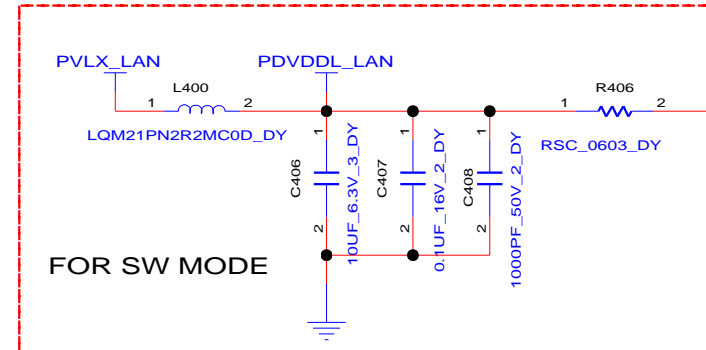


INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX DATE 21-OCT-2002 SHEET 19 of 70			



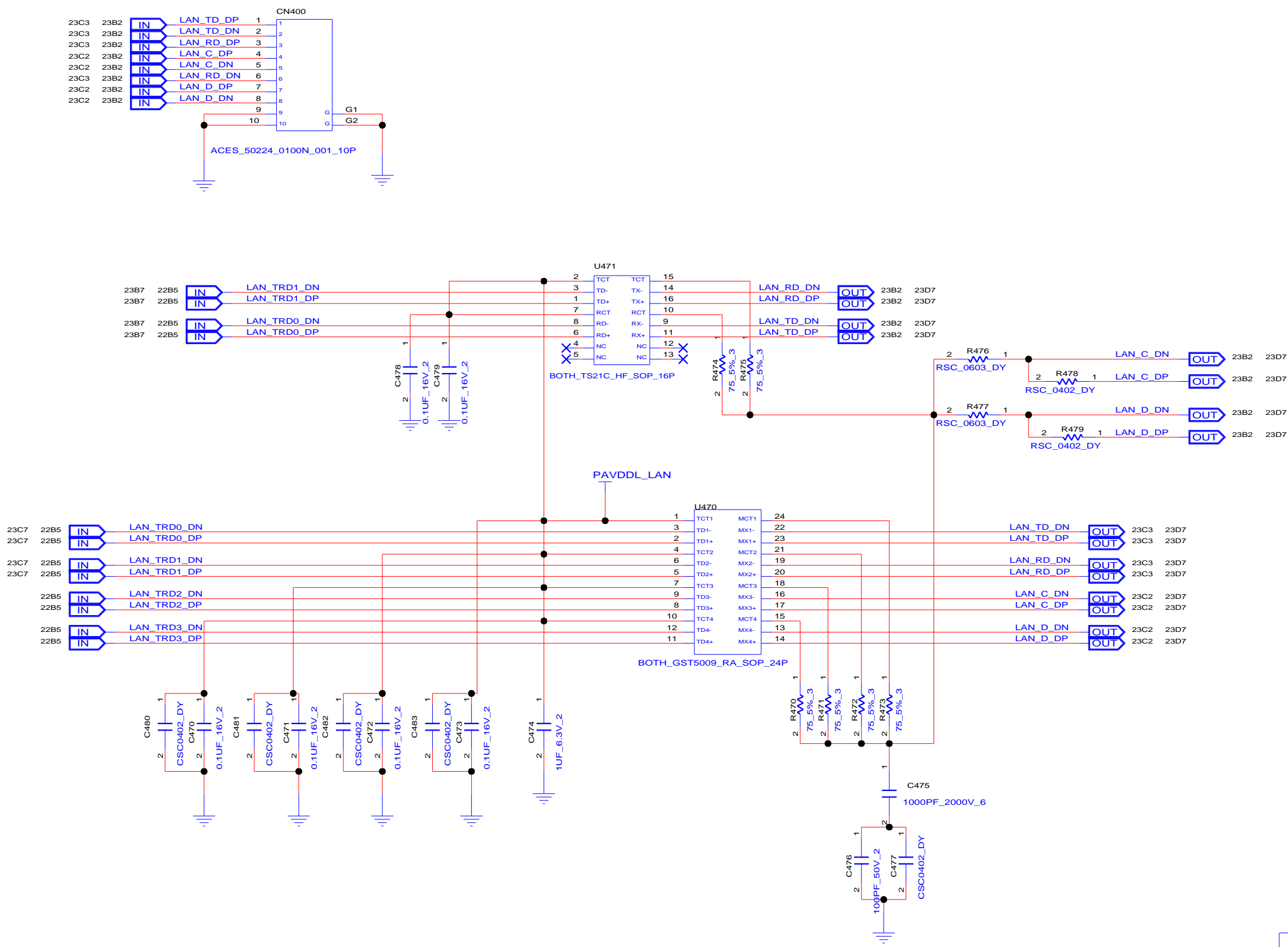
REFERENCE 300~389(KBC)





<http://sualaptop365.edu.vn>

REFERENCE 400~499(LAN)



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE
A3

CODE
CS

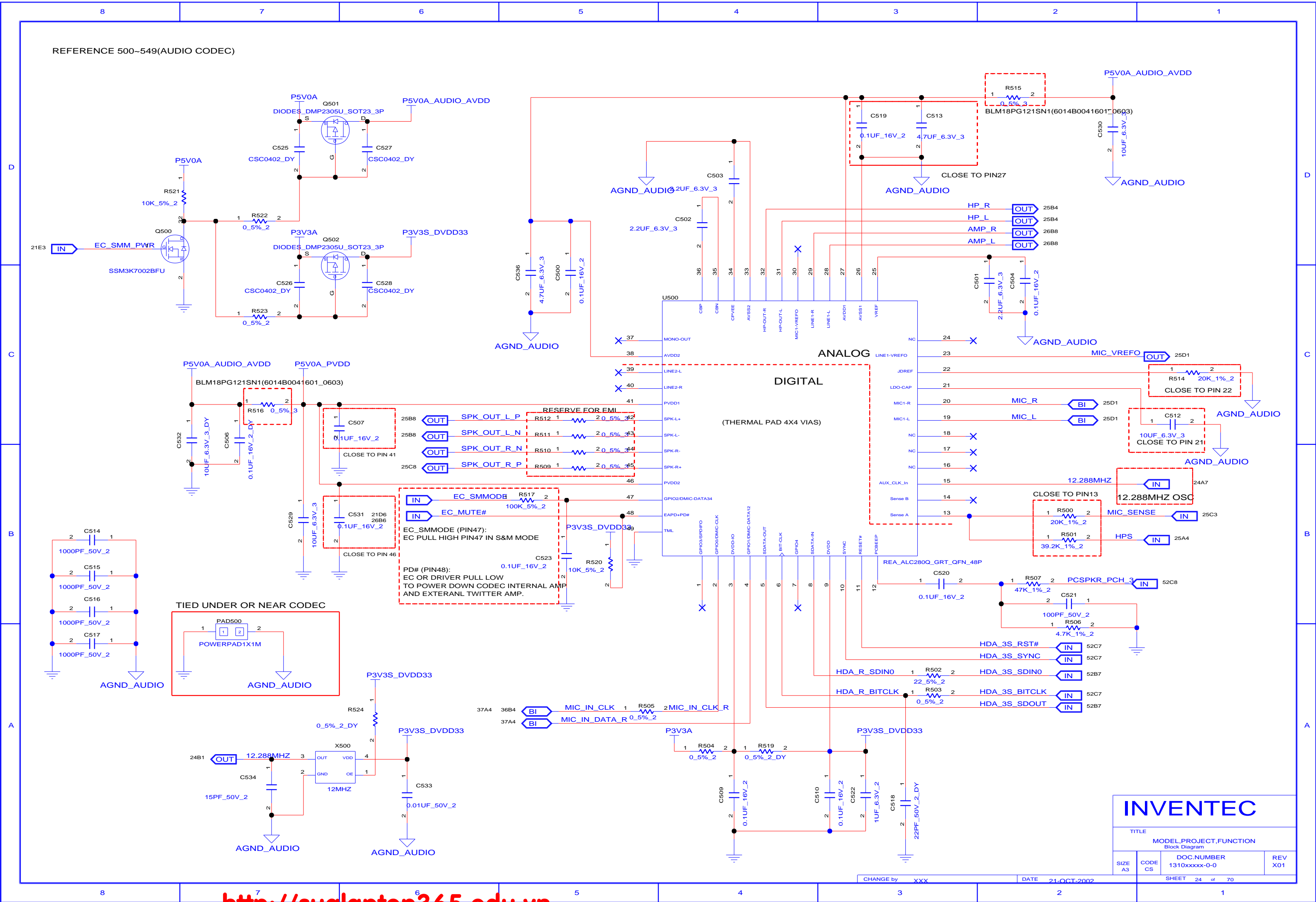
DOC.NUMBER
1310xxxx-0-0

REV
X01

CHANGE by
XXX

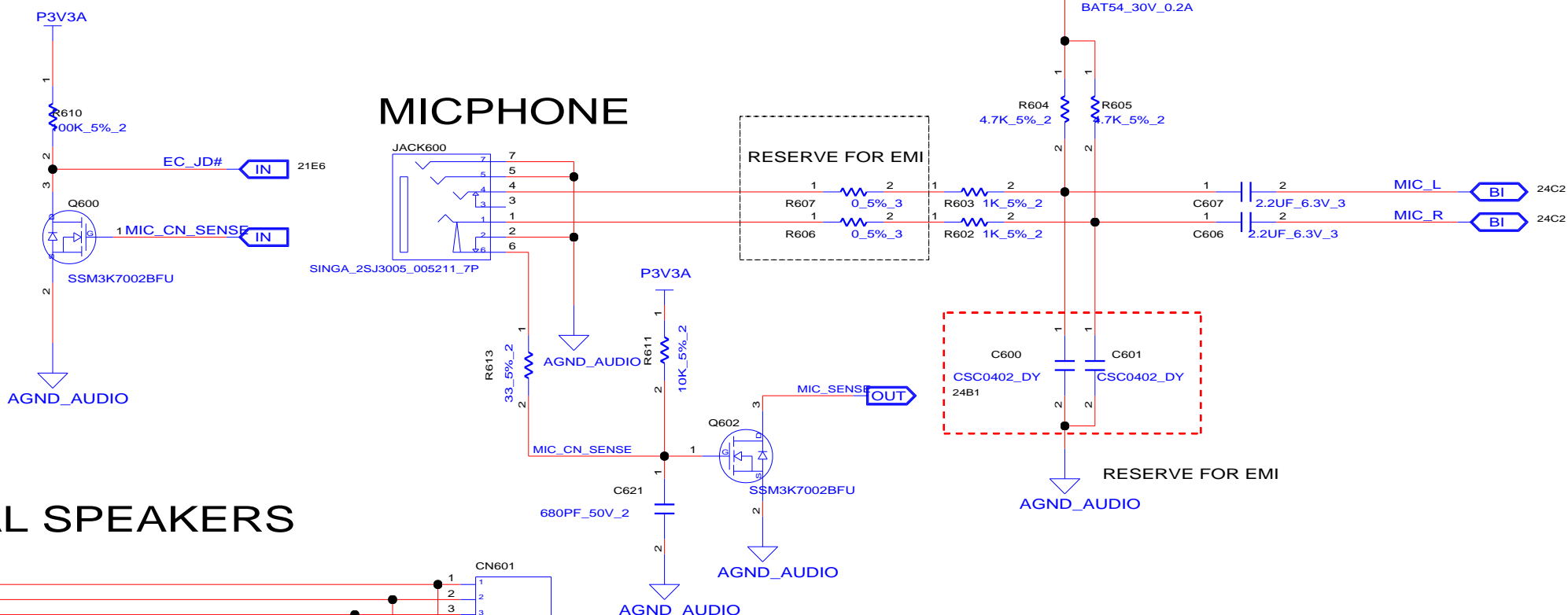
DATE
21-OCT-2002

SHEET
23 of 70

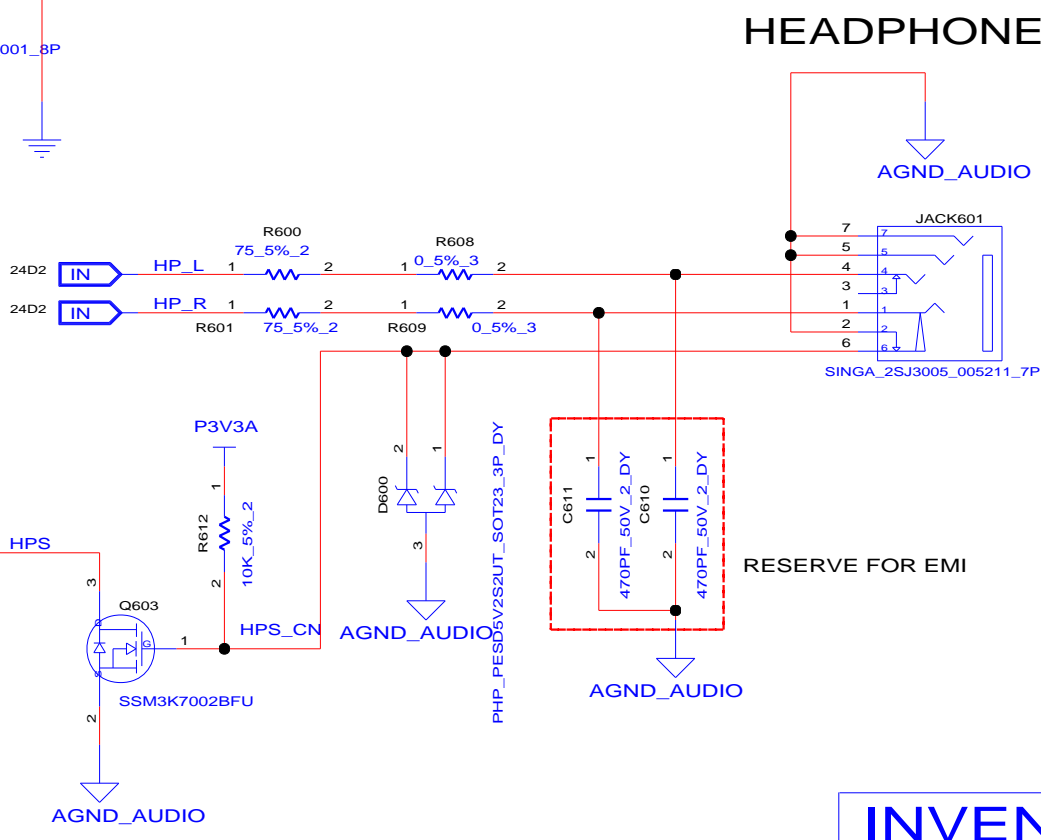
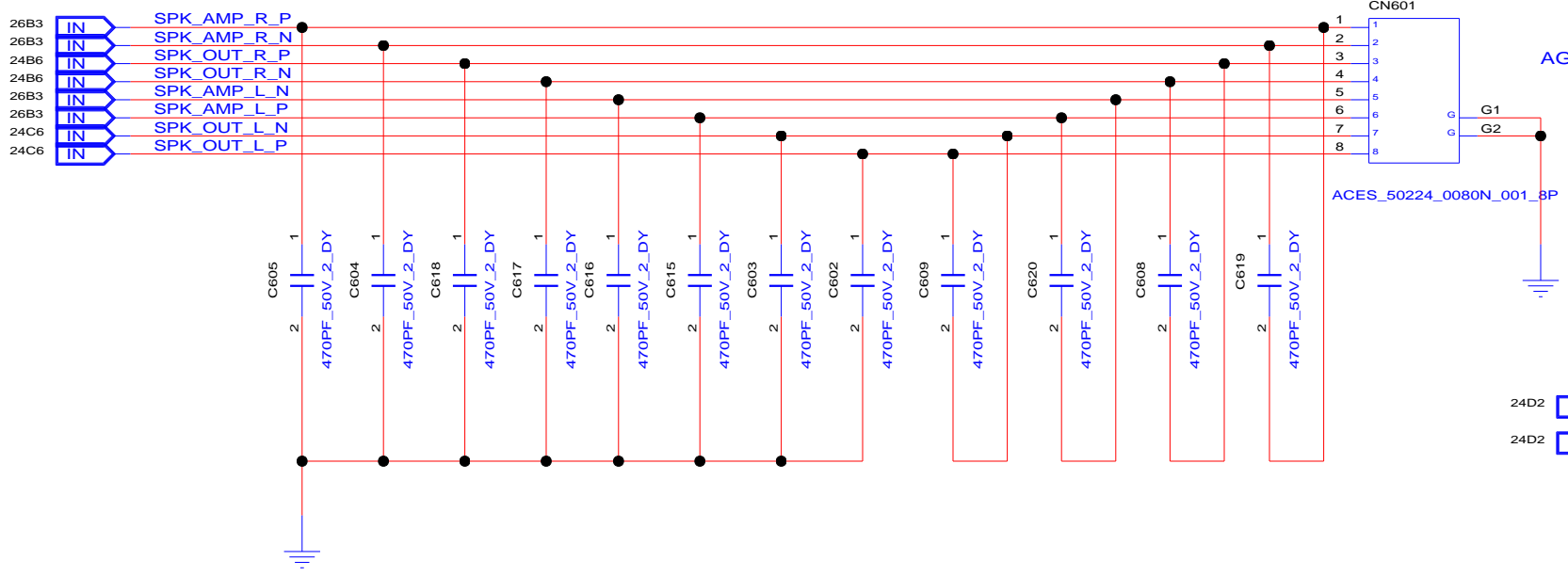


REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



INTERNAL SPEAKERS



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
------------	------------	----------------------------	------------

CHANGE by XXX DATE 21-OCT-2002

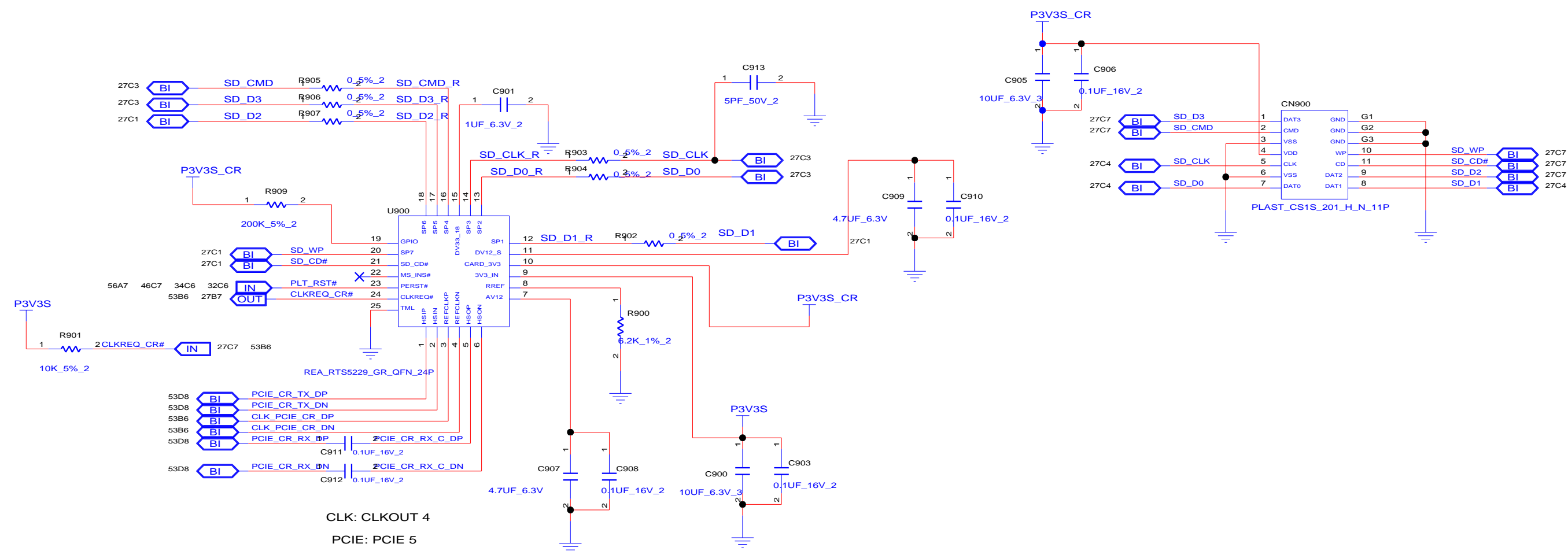
SHEET 25 of 70

A



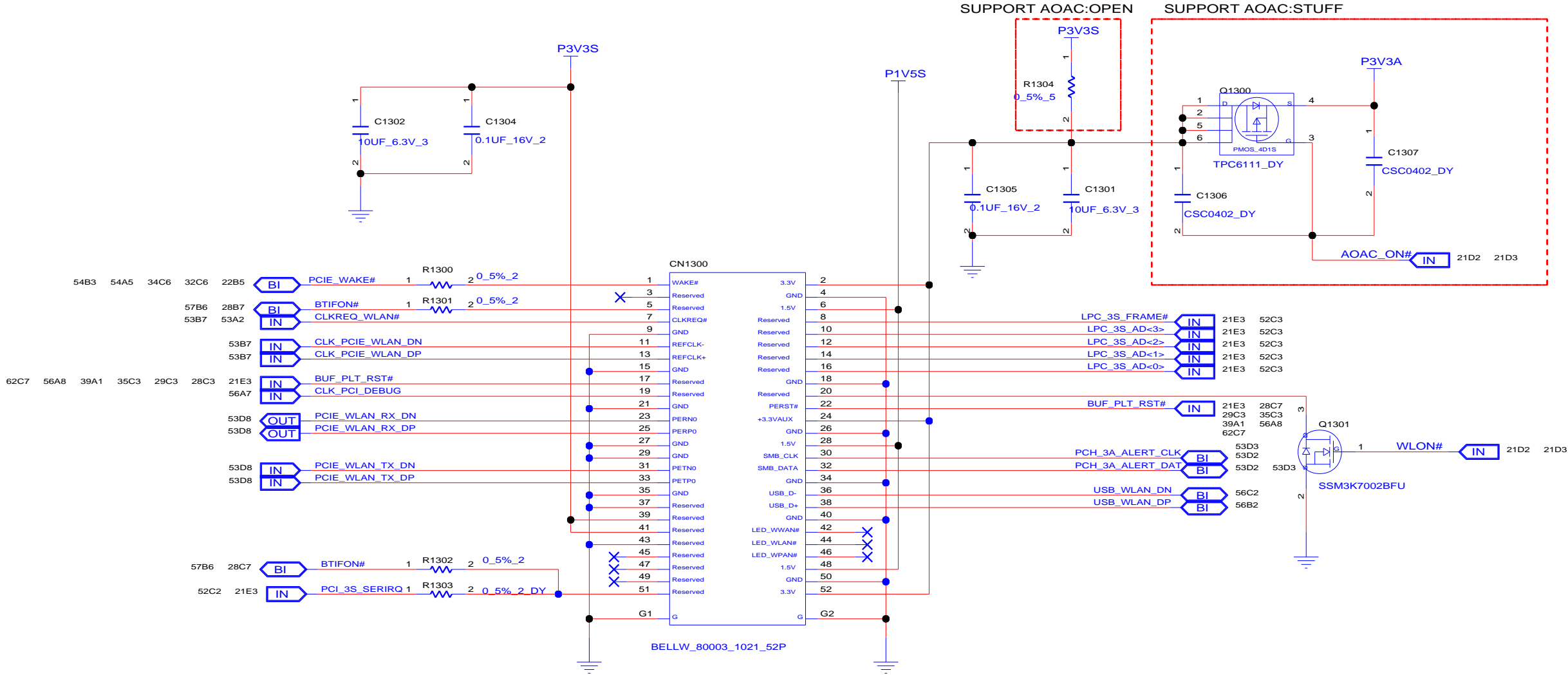
INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002
-----------	-----	------	-------------



CLK: CLKOUT 4
PCIE: PCIE 5

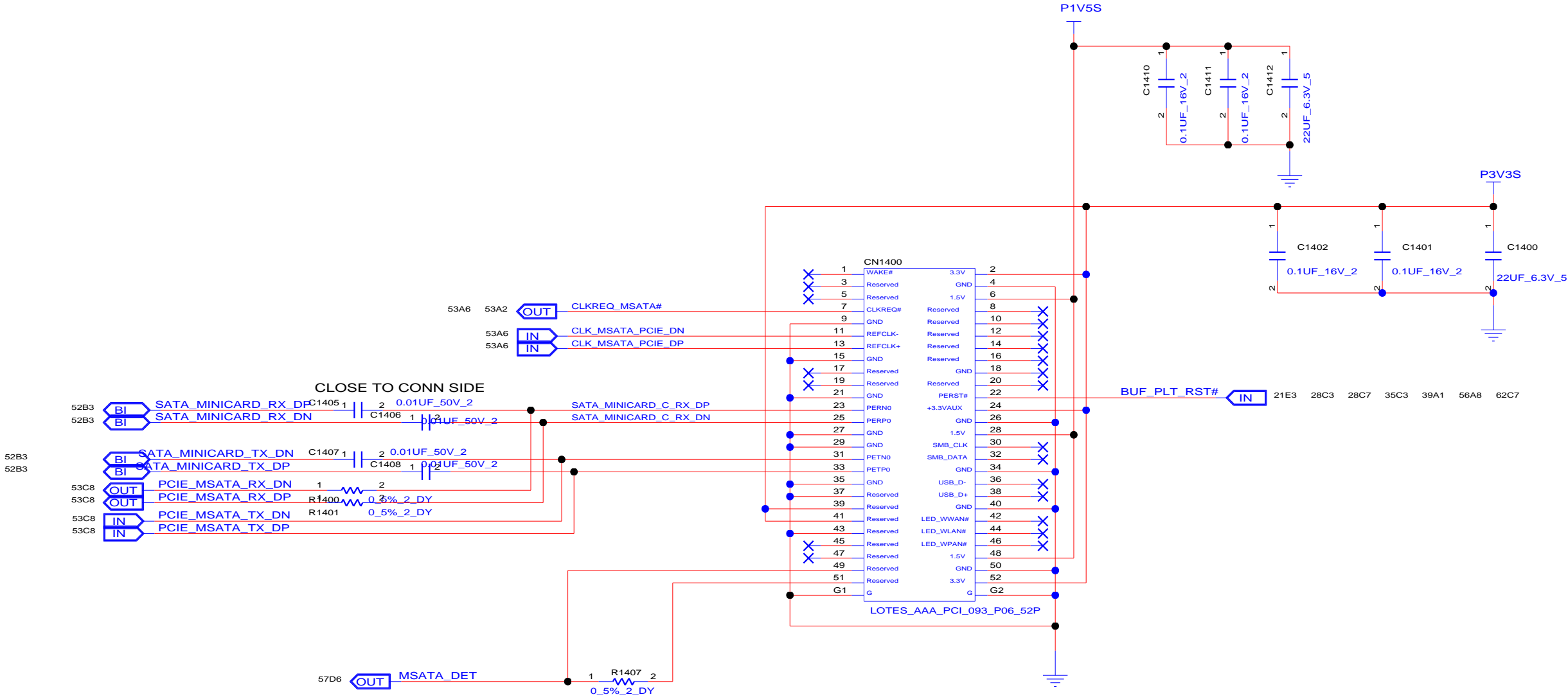
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01



MINI CARD 1(WLAN)

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

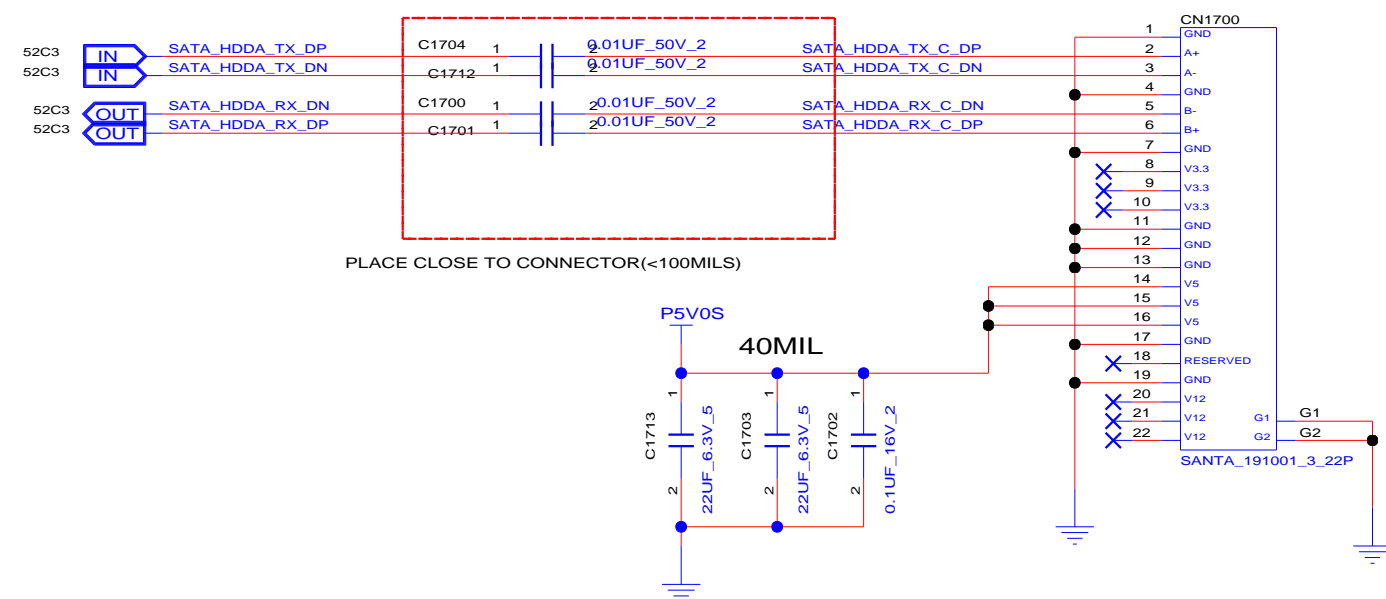
REFERENCE 1400~1499(3G)



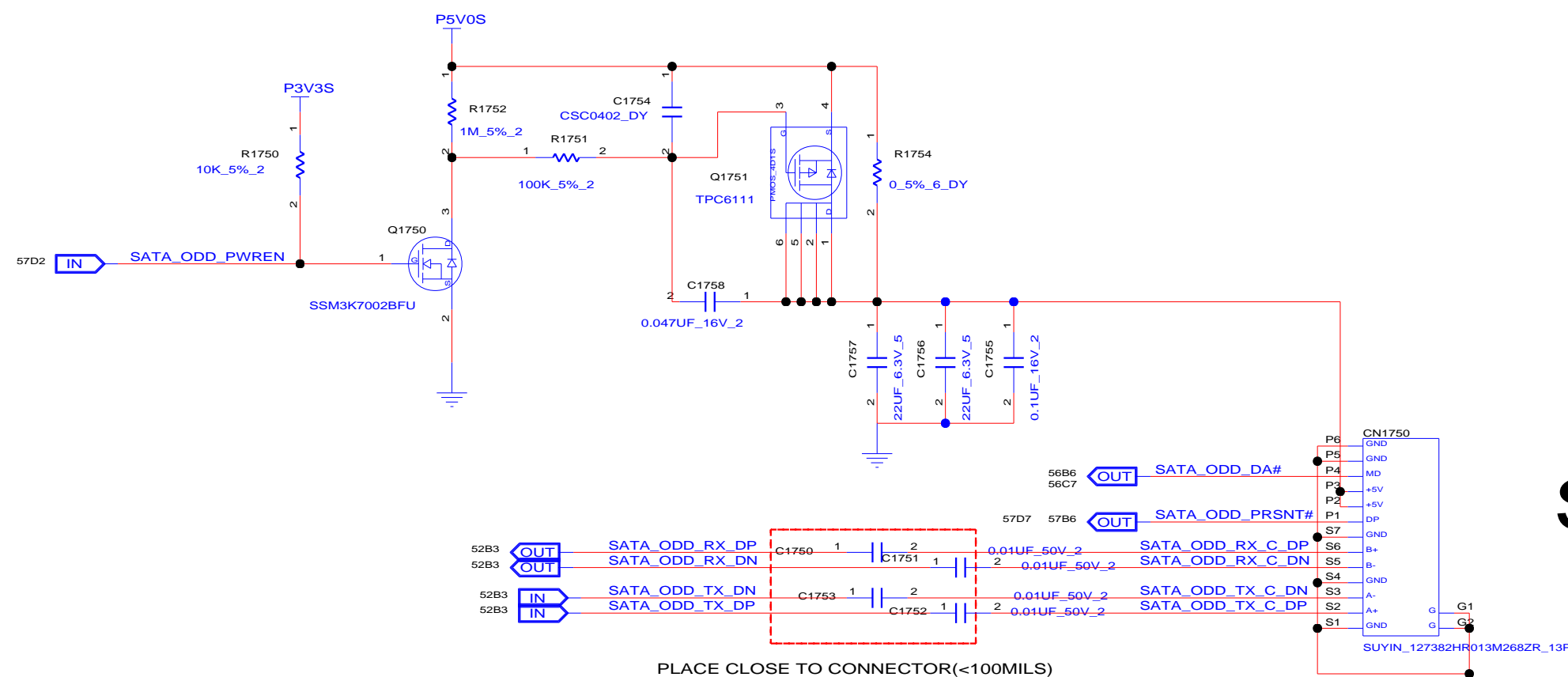
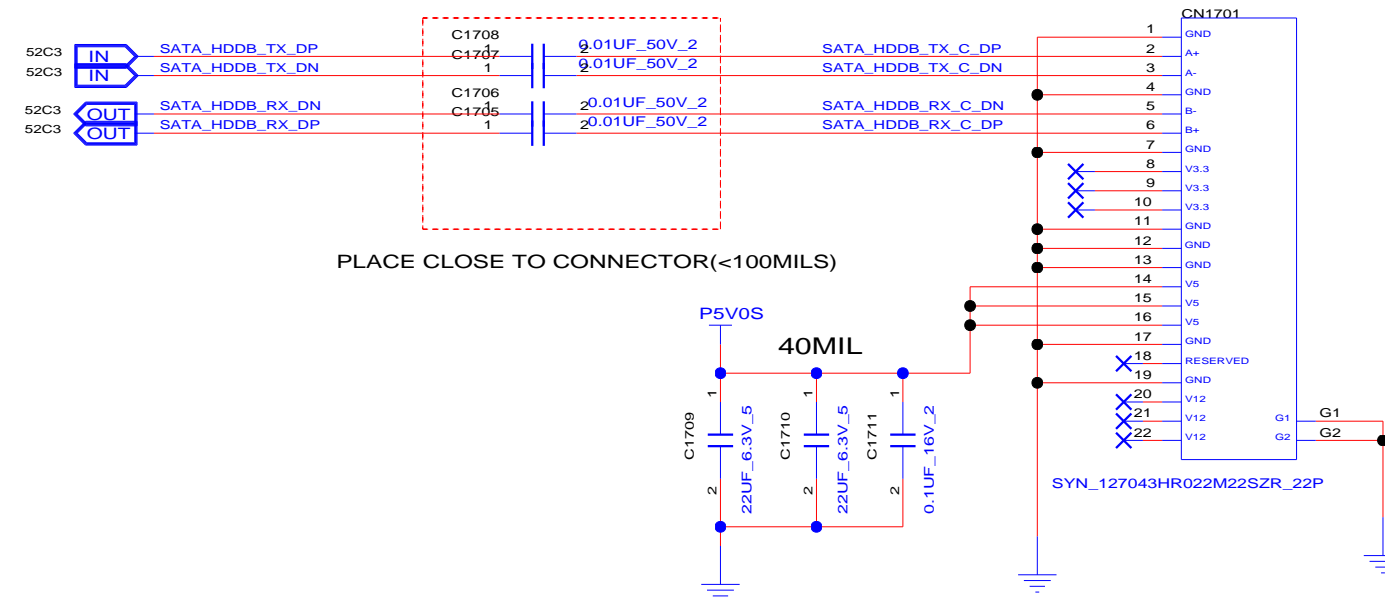
8		7		6		5		4		3		2		1	
REFERENCE 2650~2999(RESERVE)															
D														D	
C														C	
B														B	
A														A	
8		7		6		5		4		3		2		1	
CHANGE by XXX										DATE 21-OCT-2002		SHEET 30 of 70			
SIZE A3		CODE CS		DOC.NUMBER 1310xxxx-0-0						REV X01					
INVENTEC															
TITLE															
MODEL,PROJECT,FUNCTION Block Diagram															

REFERENCE 1700~1749(HDD)
REFERENCE 1750~1799(ODD)

SATA HDD A



SATA HDD B



SATA ODD

INVENTEC

TITLE MODEL,PROJECT,FUNCTION
Block Diagram

SIZE CODE DOC.NUMBER REV
A3 CS 1310xxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 31 of 70

REFERENCE 2000~2099(USB)

D

C

B

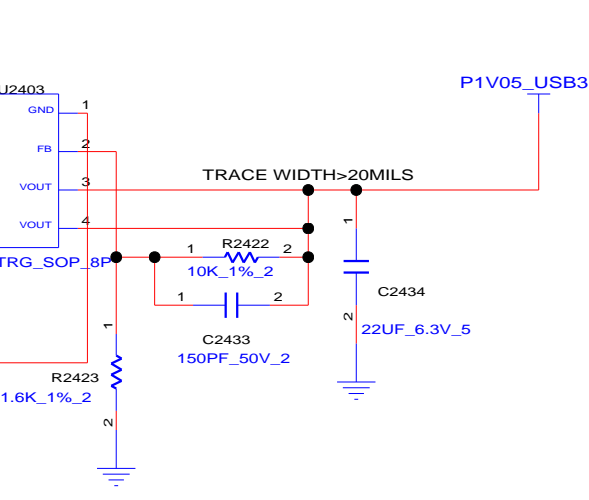
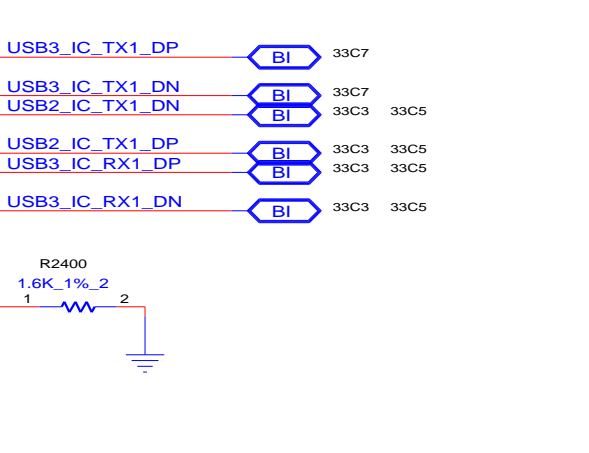
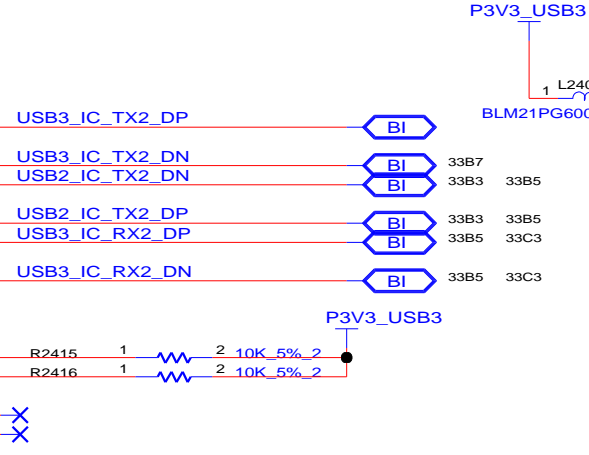
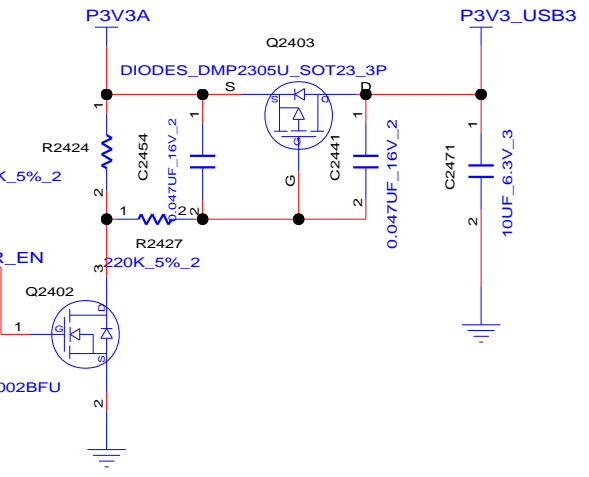
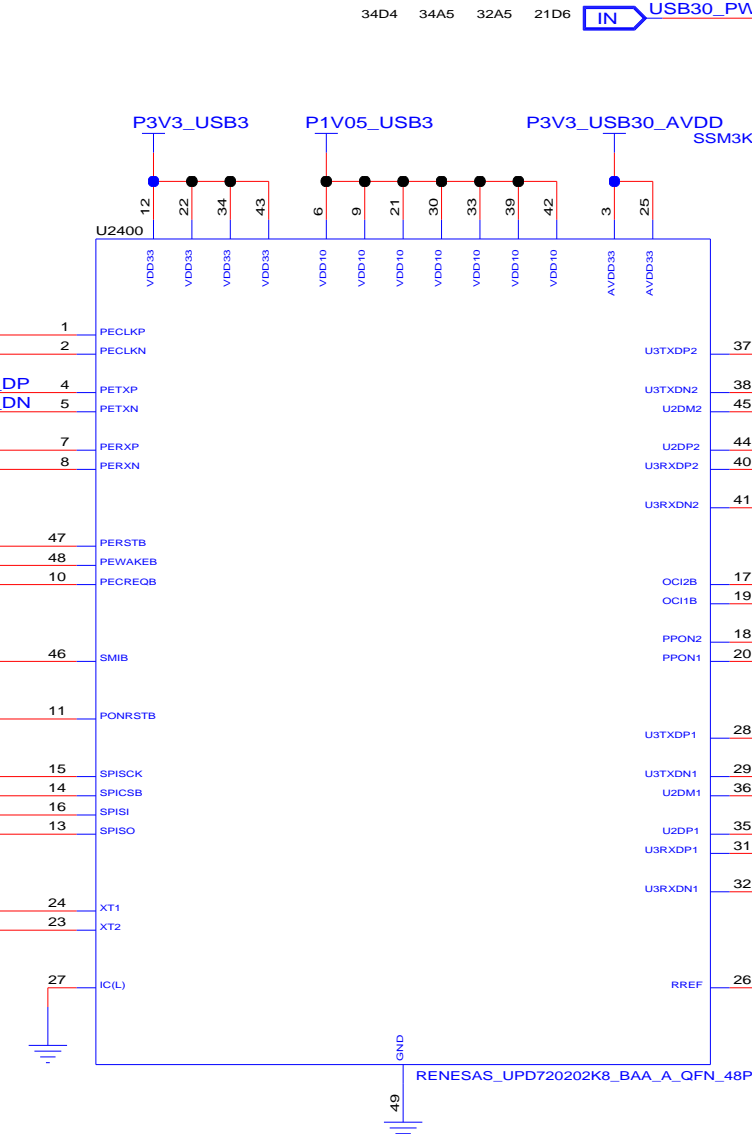
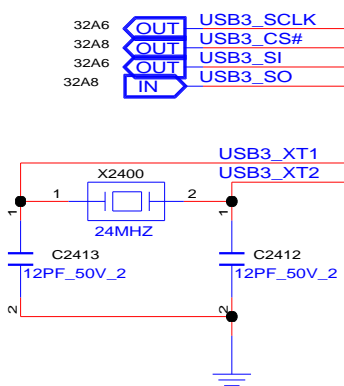
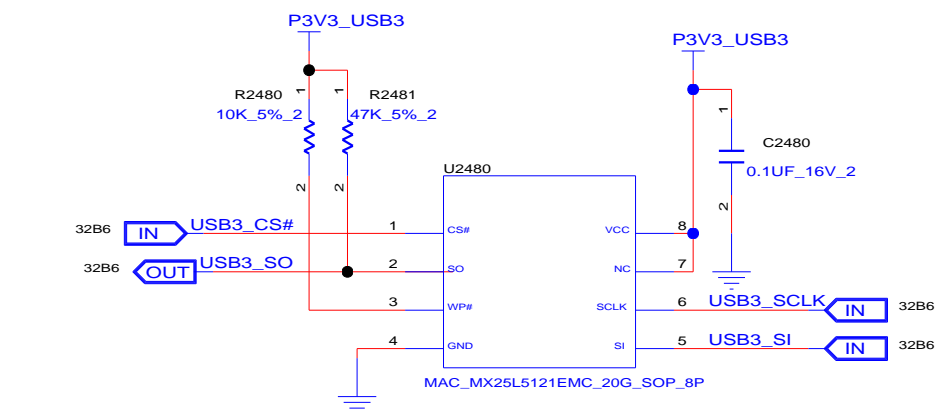
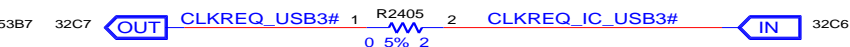
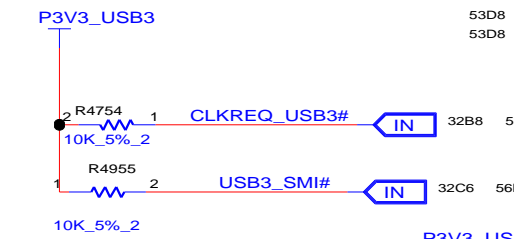
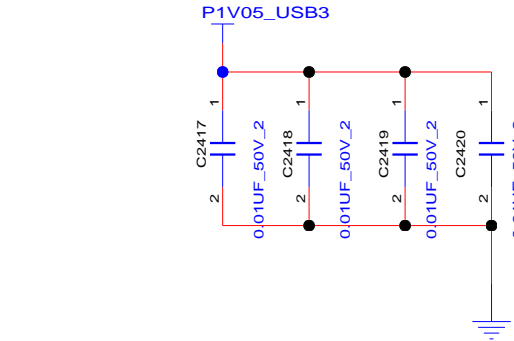
A

D

C

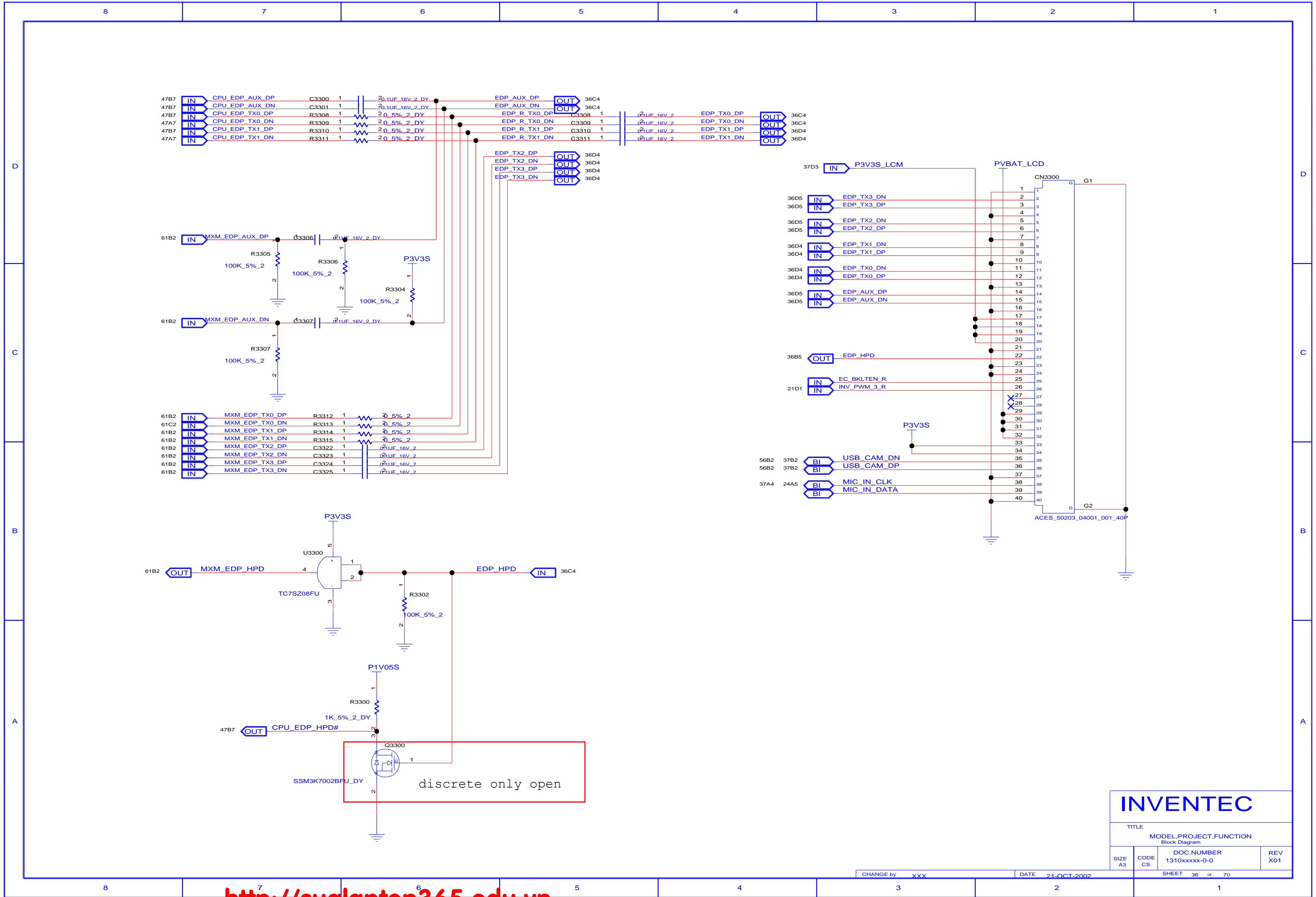
B

A



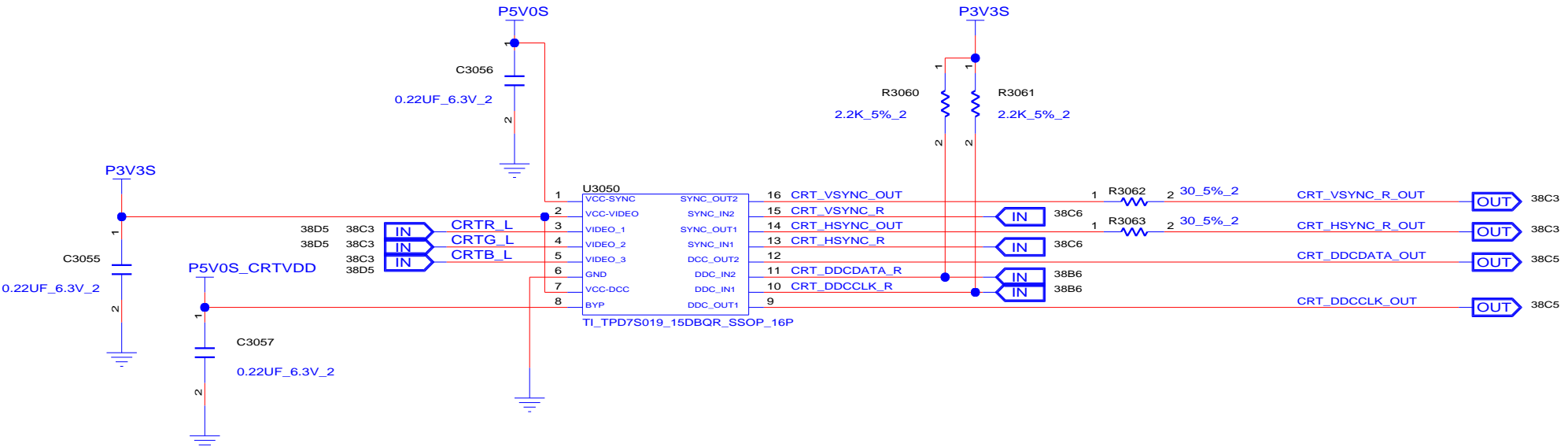
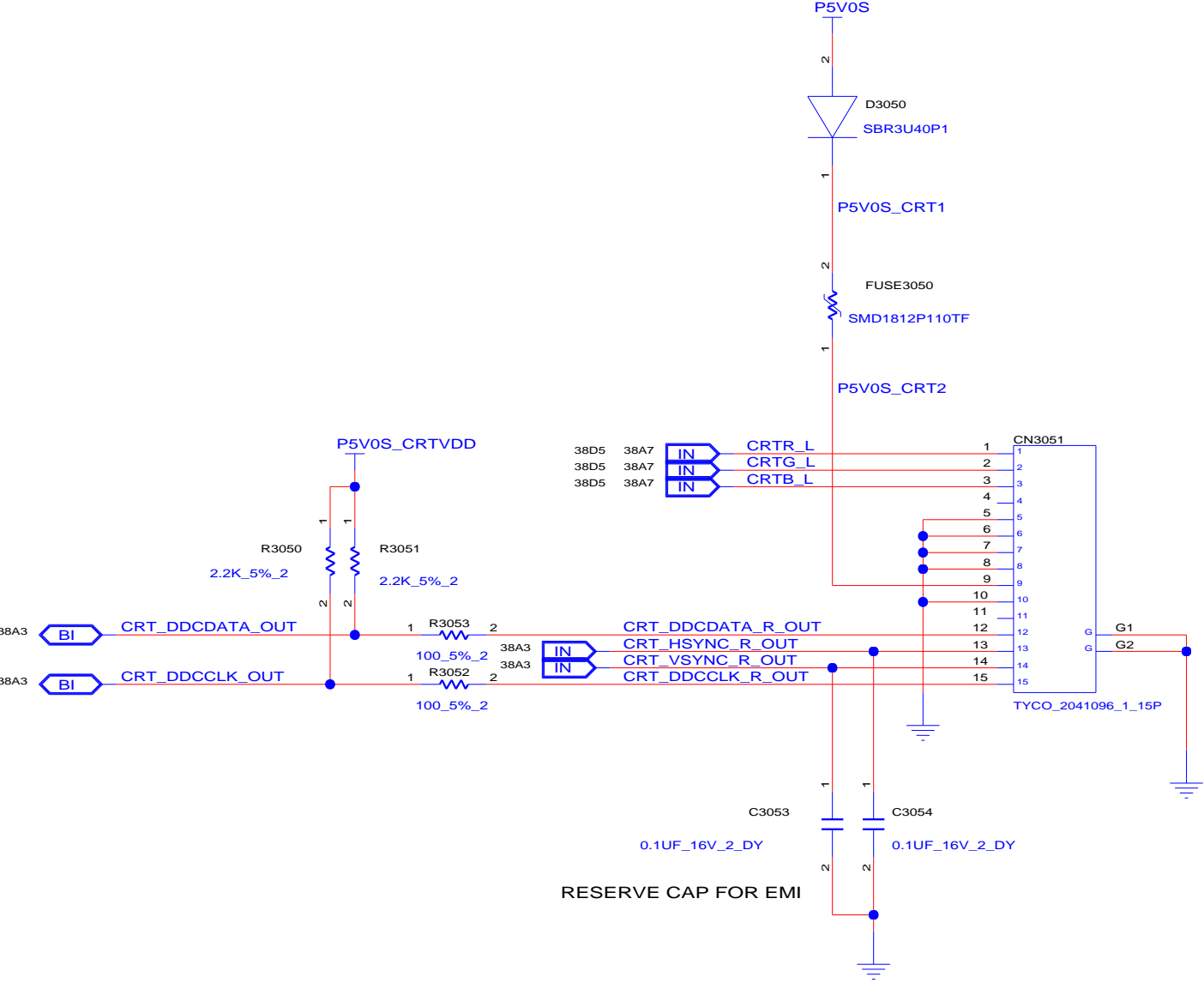
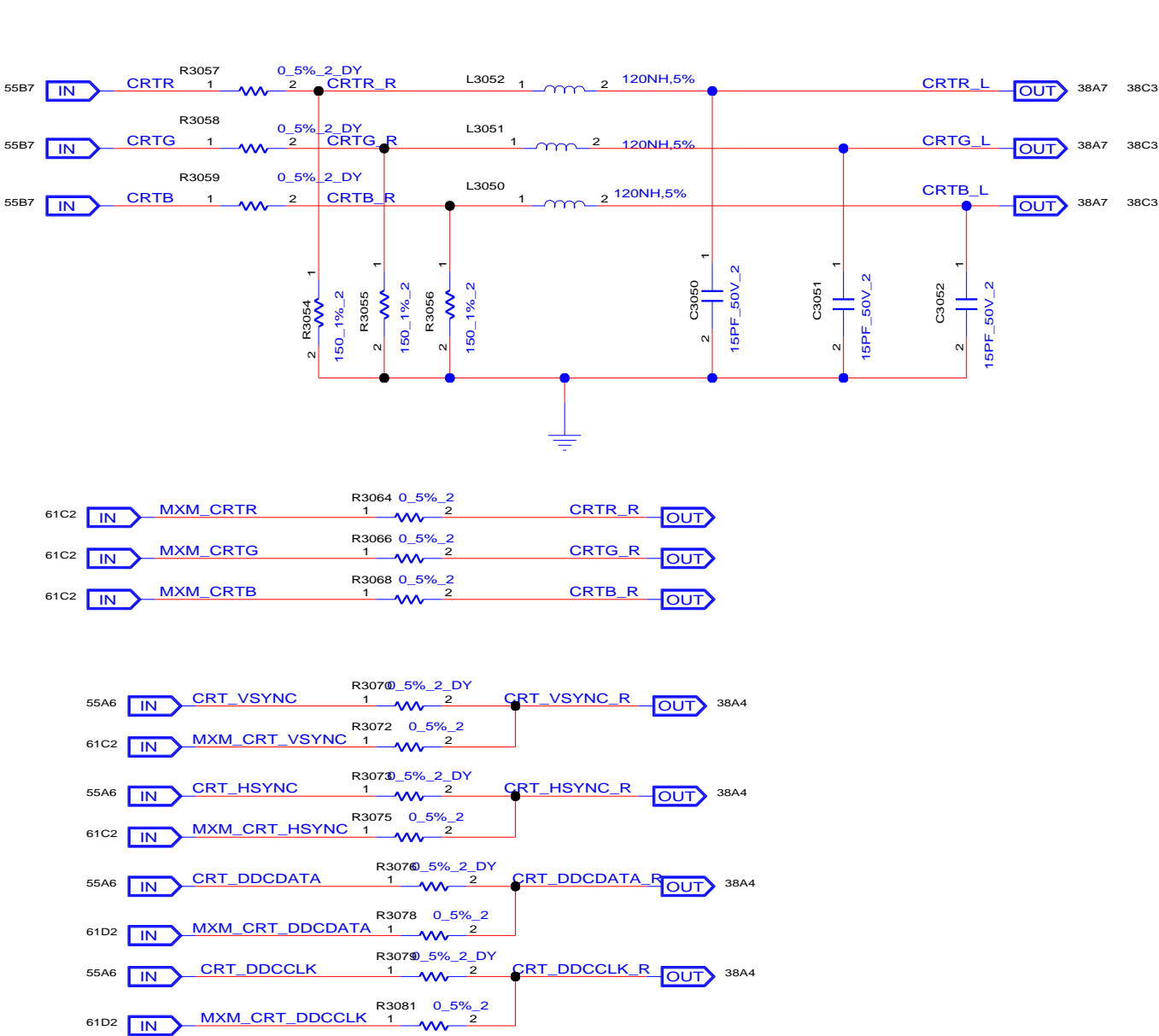
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	SHEET
XXX		21-OCT-2002	32 of 70





INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01

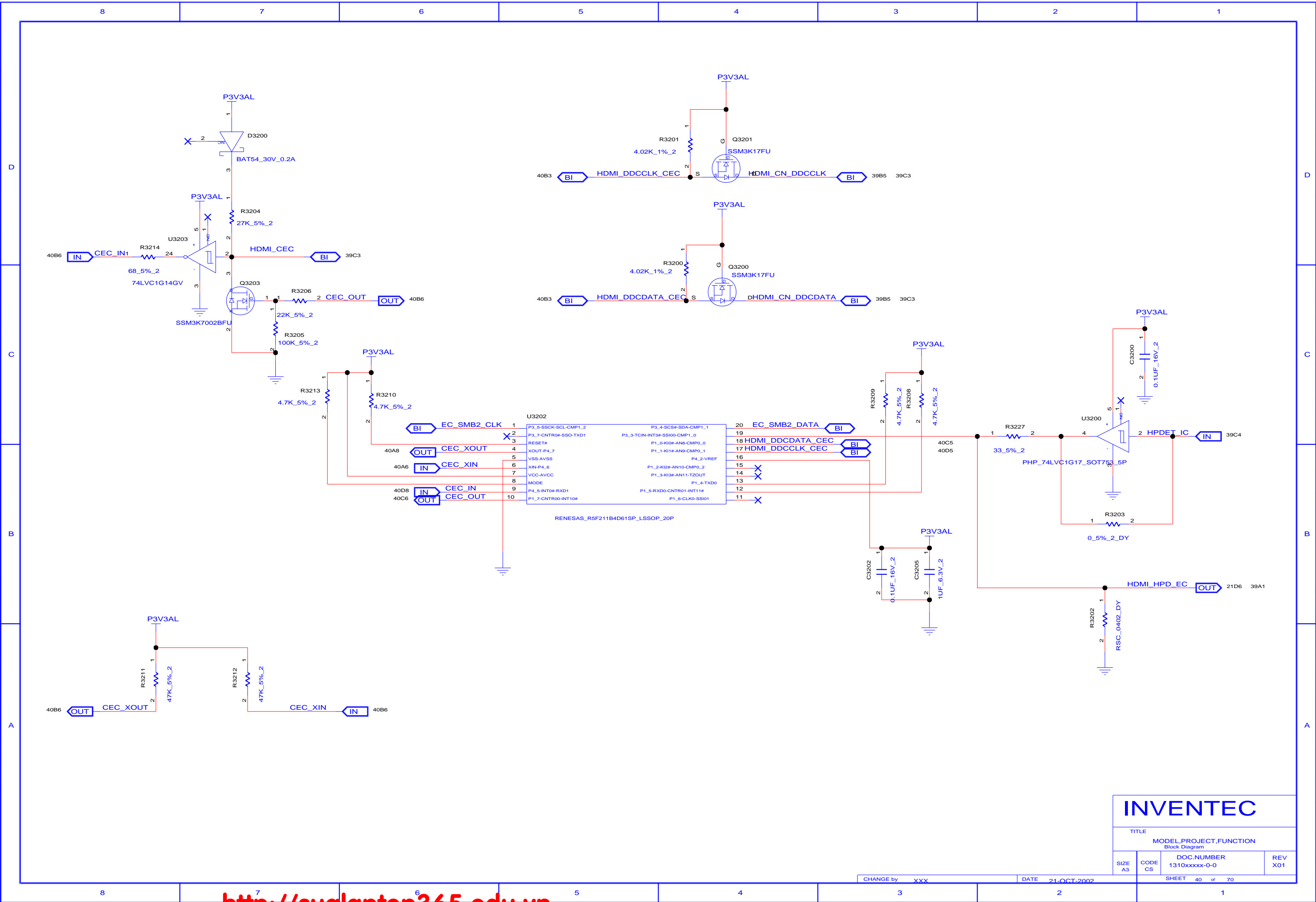
REFERENCE 3050~3099(CRT)



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 38 of 70			

CHANGE by XXX DATE 21-OCT-2002



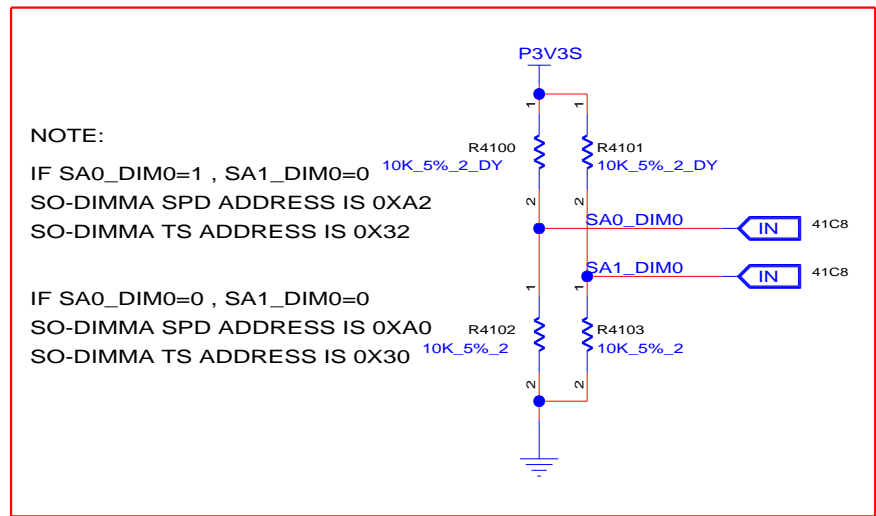
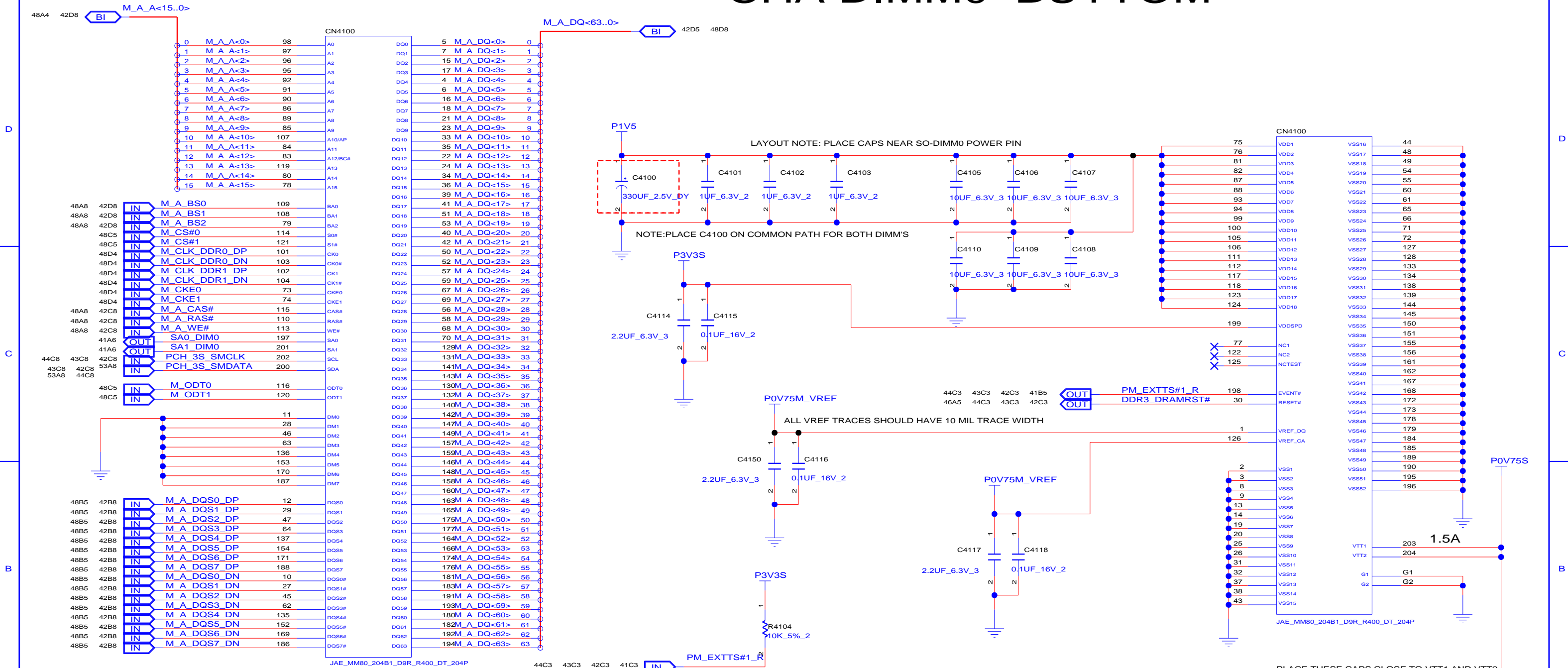


INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 40 of 70

CHA DIMM0 BUTTOM

REFERENCE 4100~4199(DDR)



INVENTEC

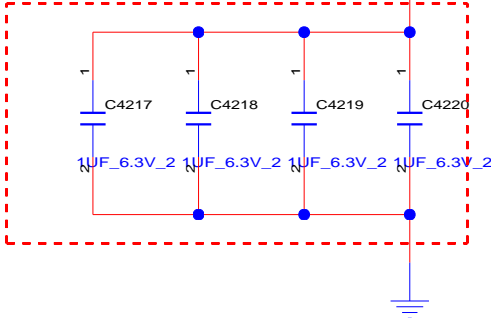
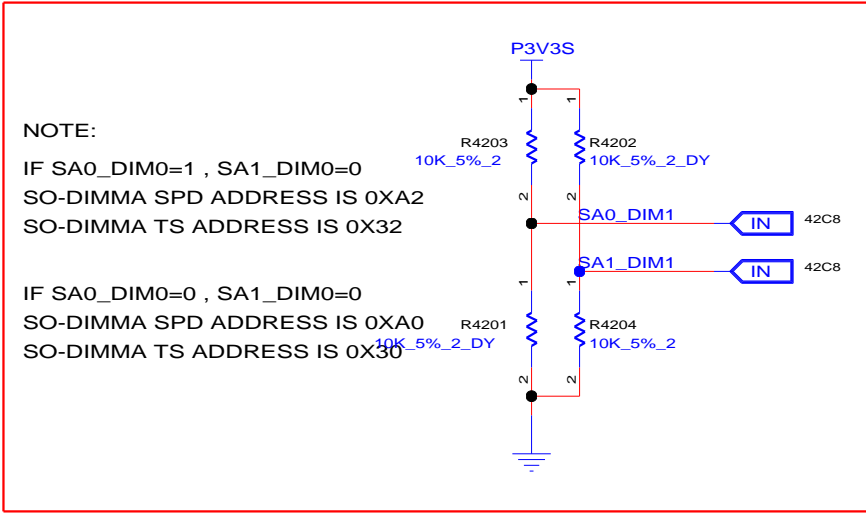
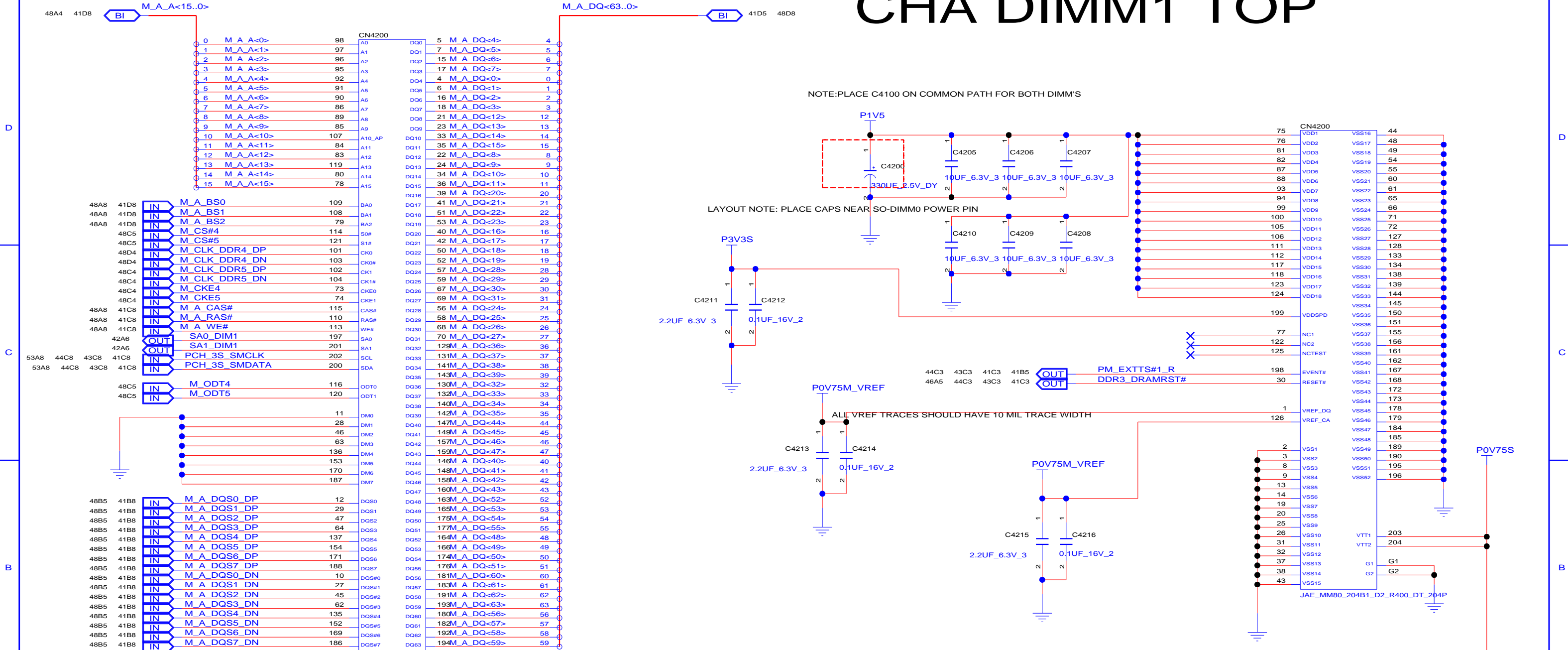
TITLE MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 41 of 70

CHA DIMM1 TOP

REFERENCE 4200~4299(DDR)



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE A3 CODE CS

DOC.NUMBER 1310xxxx-0-0

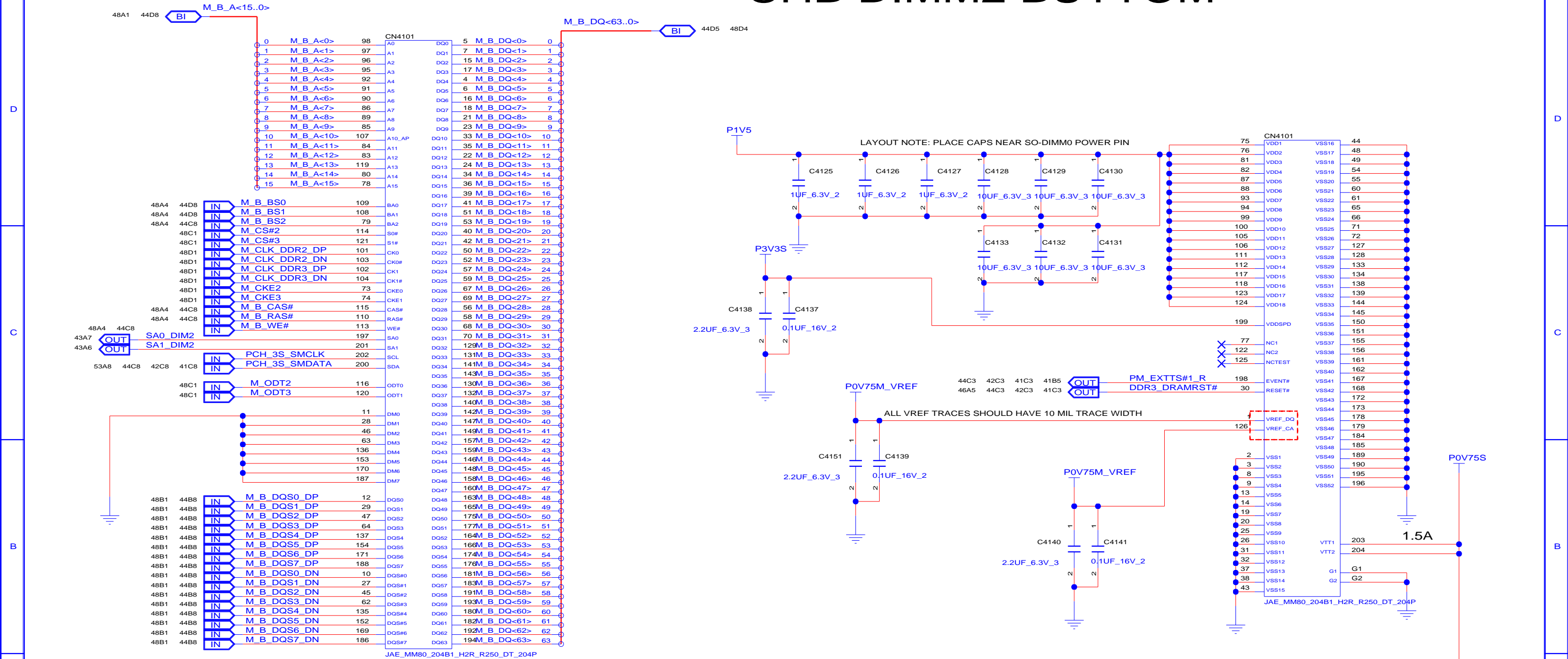
REV X01

CHANGE by XXX DATE 21-OCT-2002

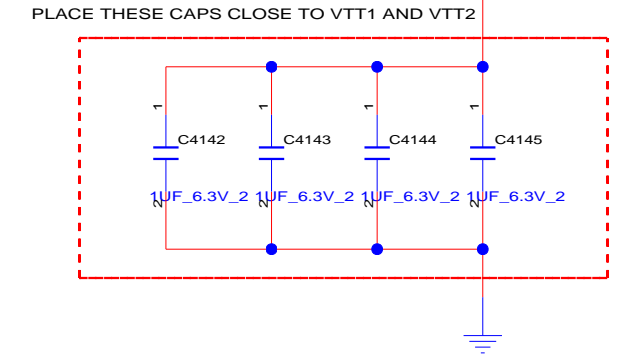
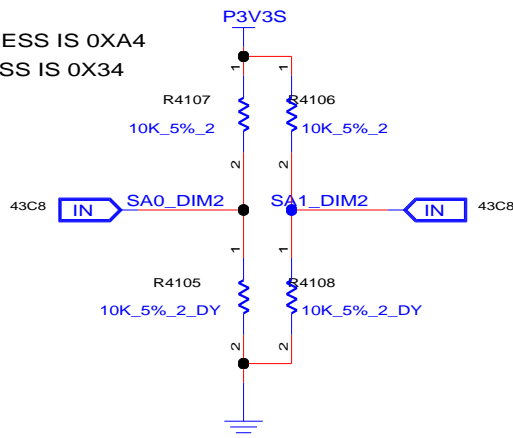
SHEET 42 of 70

REFERENCE 4100~4199(DDR)

CHB DIMM2 BUTTOM



NOTE:
SO-DIMMB SPD ADDRESS IS 0XA4
SO-DIMMB TS ADDRESS IS 0X34



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION
Block Diagram

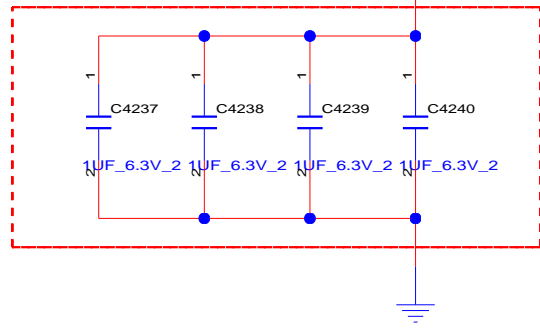
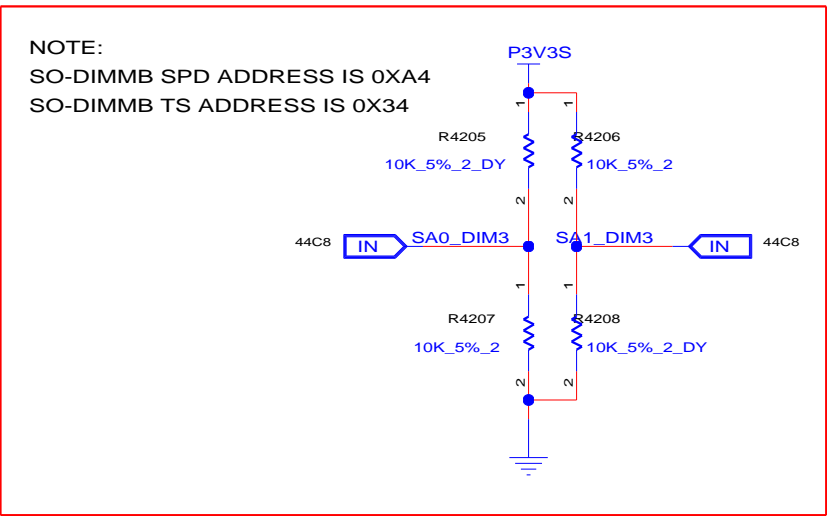
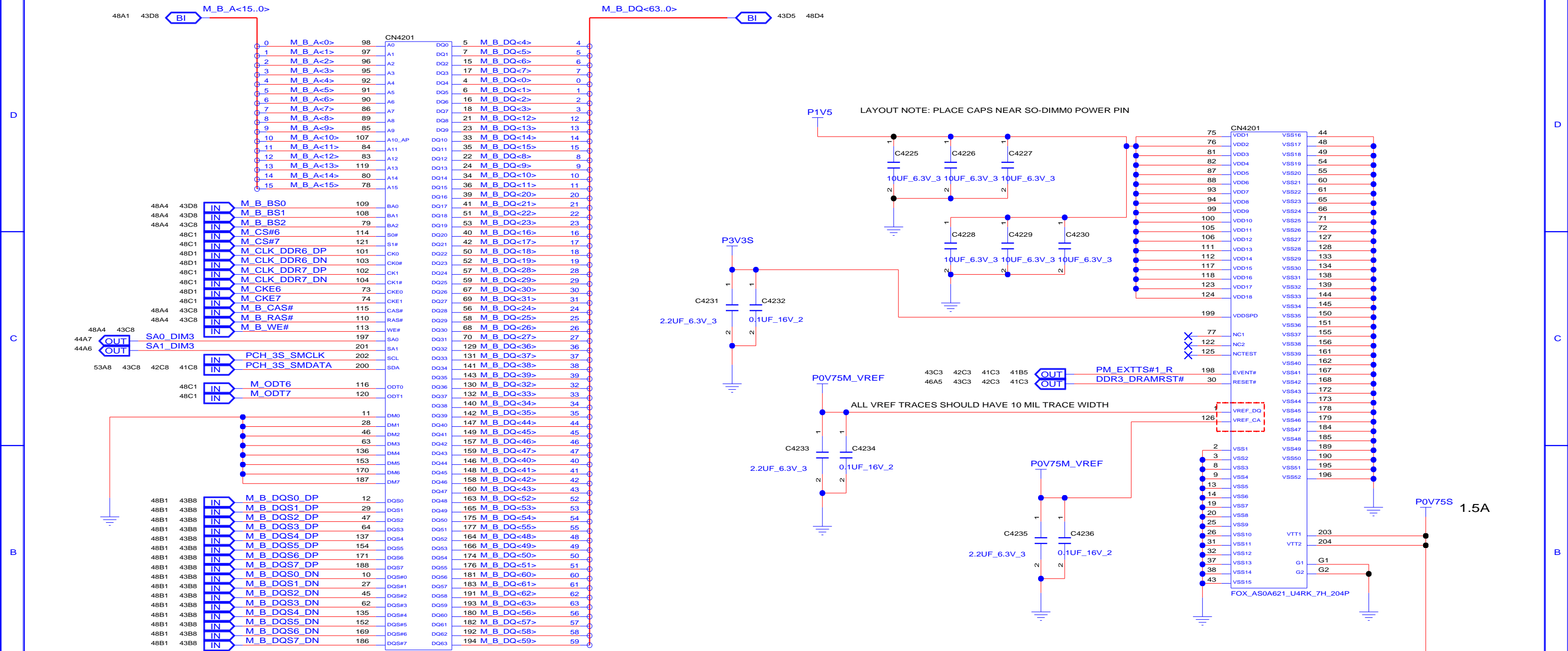
SIZE A3 CODE CS DOC.NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 43 of 70

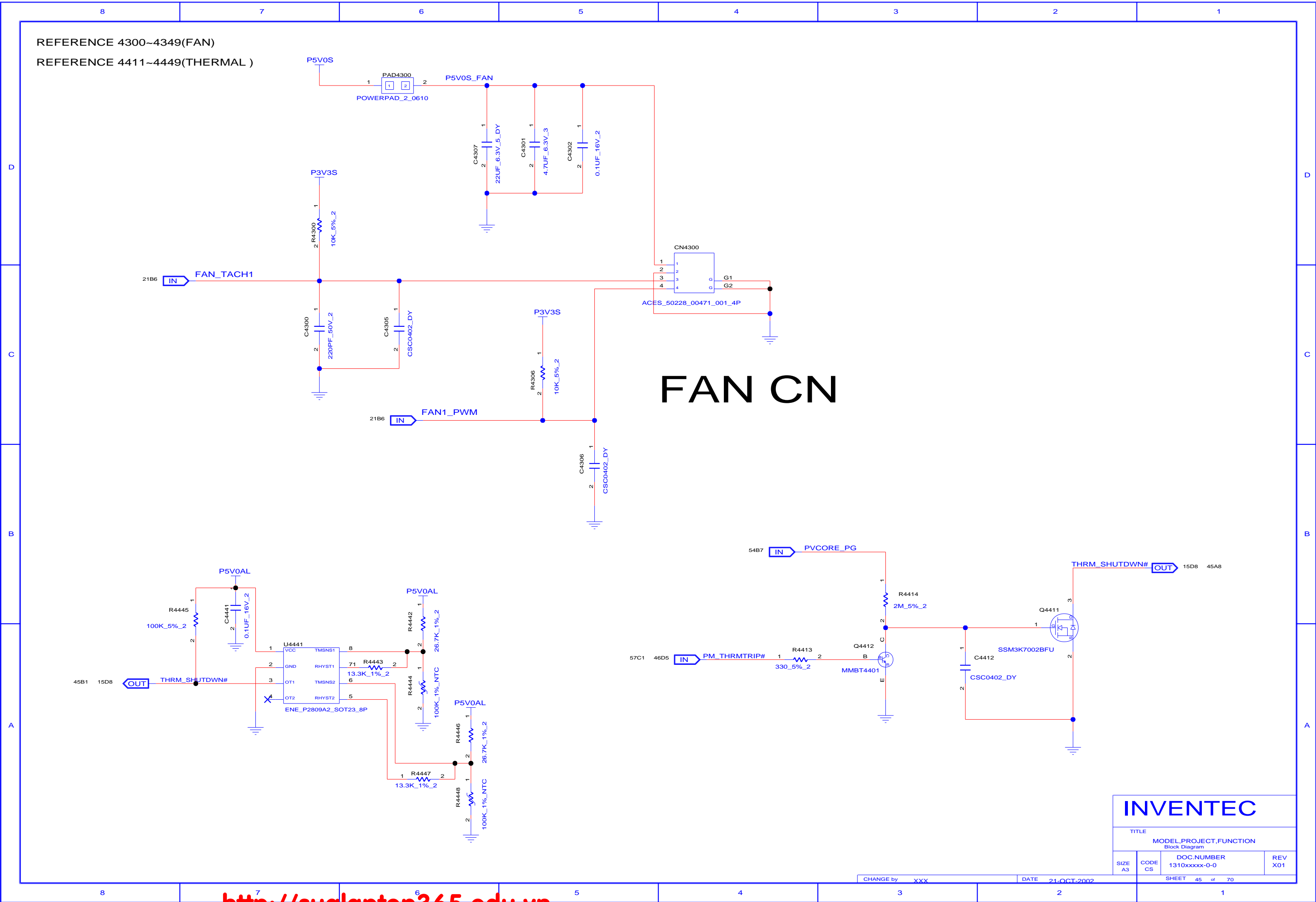
REFERENCE 4200~4299(DDR)

CHB DIMM3 TOP



INVENTEC

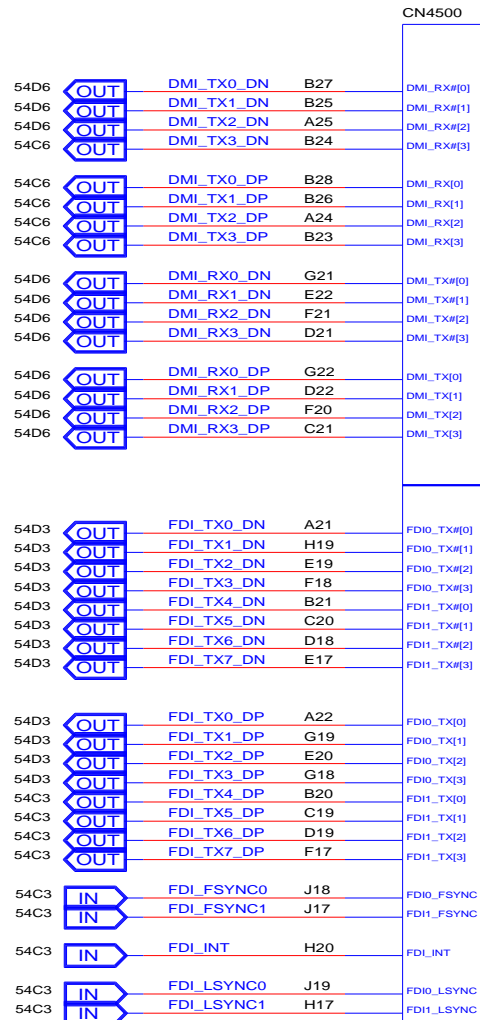
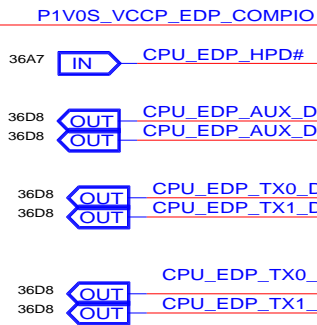
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01



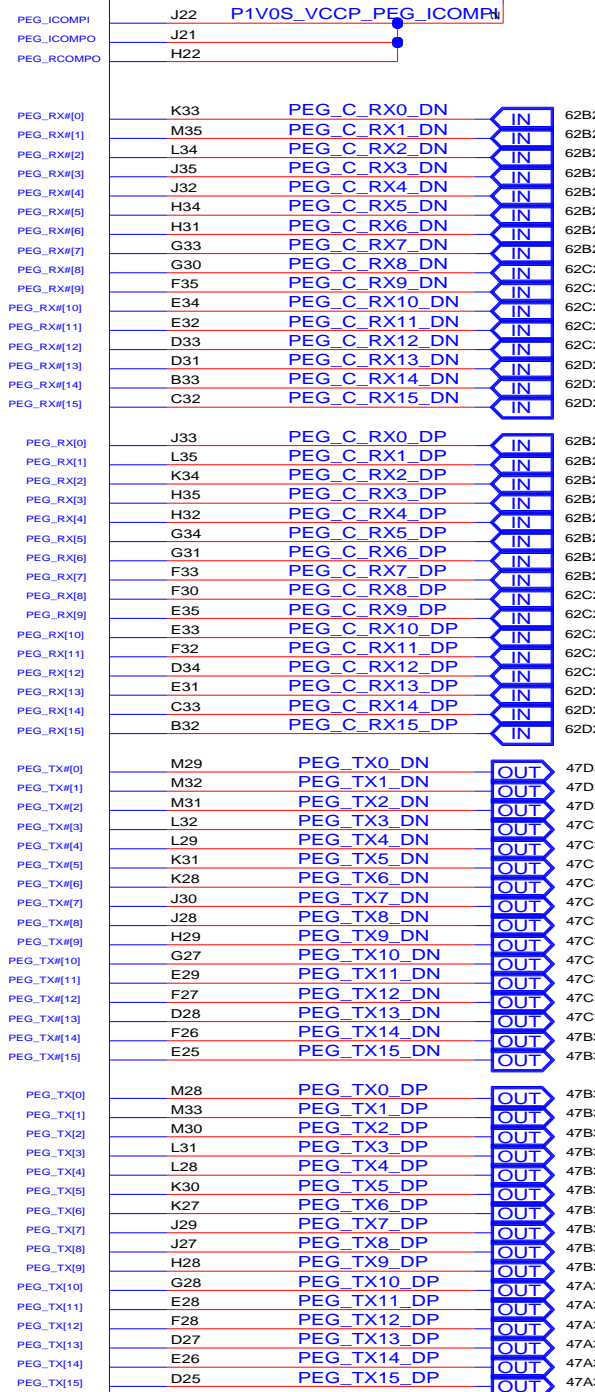
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

REFERENCE 4500~4699(CPU)



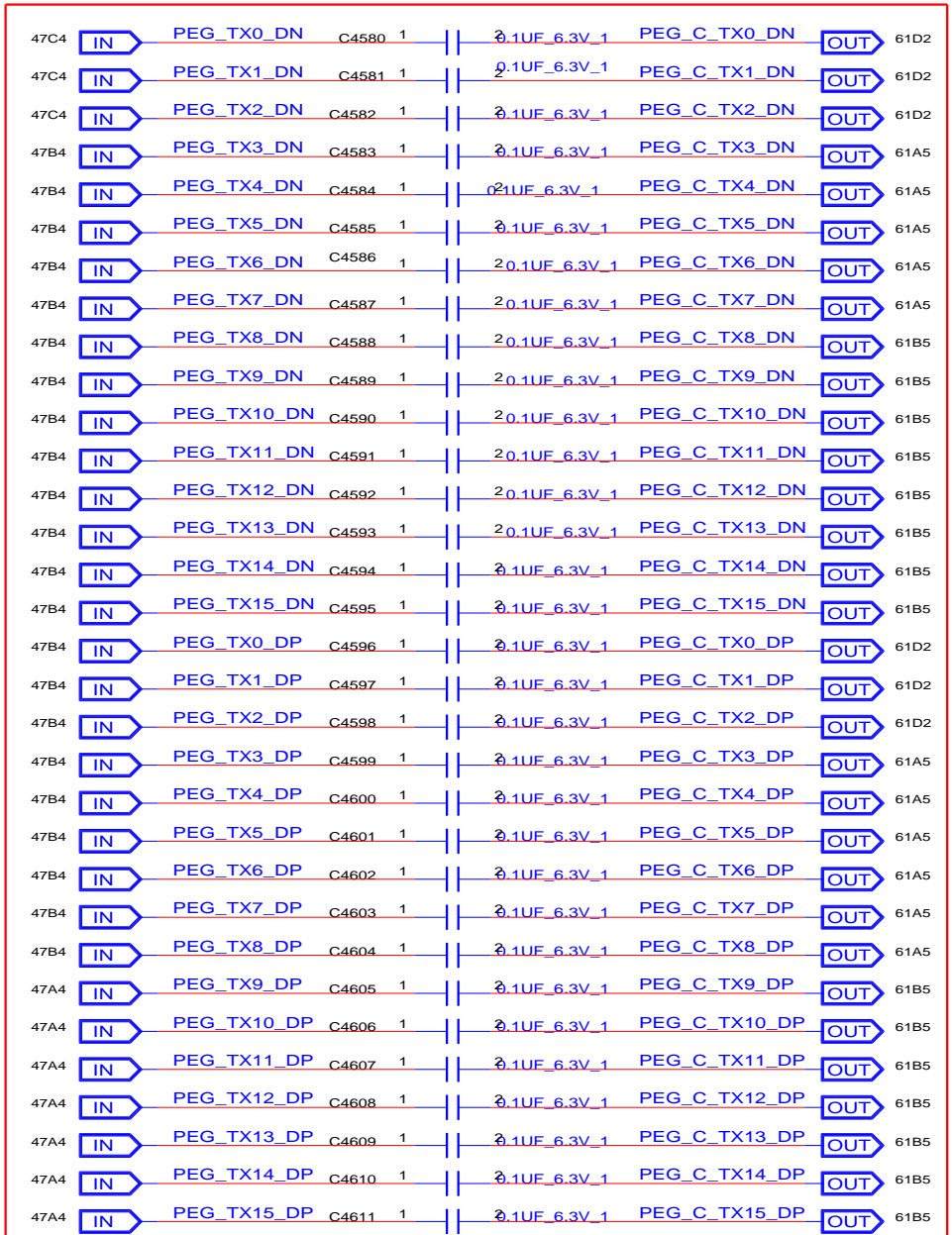
PCI EXPRESS* - GRAPHICS



CAD NOTE: PEG_IOMPI AND RCOMP signals
SHOULD BE SHORTED AND ROUTED WITH
- MAX LENGTH = 500 MILS
- TYPICAL IMPEDANCE = 43 MOHMS

PEG_IOMPO signals SHOULD BE ROUTED WITH
- MAX LENGTH = 500 MILS
- TYPICAL IMPEDANCE = 14.5 MOHMS

CLOSE TO CPU



CAD NOTE: DP_COMPIO AND ICOMPO signals
SHOULD BE SHORTED NEAR BALLS AND ROUTED WITH
- TYPICAL IMPEDANCE < 25 MOHMS

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 47 of 70

REFERENCE 4500~4699(CPU)

SOCKET,CPU,989P,TIN,3.0MM,STR,SMD,TR

CN4500

42D5 41D5 BI M_A_DQ<63..0>

0	M_A_DQ<0>	C5	SA_DQ[0]
1	M_A_DQ<1>	D5	SA_DQ[1]
2	M_A_DQ<2>	D3	SA_DQ[2]
3	M_A_DQ<3>	D2	SA_DQ[3]
4	M_A_DQ<4>	D6	SA_DQ[4]
5	M_A_DQ<5>	C6	SA_DQ[5]
6	M_A_DQ<6>	C2	SA_DQ[6]
7	M_A_DQ<7>	C3	SA_DQ[7]
8	M_A_DQ<8>	F10	SA_DQ[8]
9	M_A_DQ<9>	F8	SA_DQ[9]
10	M_A_DQ<10>	G10	SA_DQ[10]
11	M_A_DQ<11>	G9	SA_DQ[11]
12	M_A_DQ<12>	F9	SA_DQ[12]
13	M_A_DQ<13>	F7	SA_DQ[13]
14	M_A_DQ<14>	G8	SA_DQ[14]
15	M_A_DQ<15>	G7	SA_DQ[15]
16	M_A_DQ<16>	K4	SA_DQ[16]
17	M_A_DQ<17>	K5	SA_DQ[17]
18	M_A_DQ<18>	K1	SA_DQ[18]
19	M_A_DQ<19>	J1	SA_DQ[19]
20	M_A_DQ<20>	J5	SA_DQ[20]
21	M_A_DQ<21>	J4	SA_DQ[21]
22	M_A_DQ<22>	J2	SA_DQ[22]
23	M_A_DQ<23>	K2	SA_DQ[23]
24	M_A_DQ<24>	M8	SA_DQ[24]
25	M_A_DQ<25>	N10	SA_DQ[25]
26	M_A_DQ<26>	N8	SA_DQ[26]
27	M_A_DQ<27>	N7	SA_DQ[27]
28	M_A_DQ<28>	M10	SA_DQ[28]
29	M_A_DQ<29>	M9	SA_DQ[29]
30	M_A_DQ<30>	N9	SA_DQ[30]
31	M_A_DQ<31>	M7	SA_DQ[31]
32	M_A_DQ<32>	AG6	SA_DQ[32]
33	M_A_DQ<33>	AG5	SA_DQ[33]
34	M_A_DQ<34>	AK6	SA_DQ[34]
35	M_A_DQ<35>	AK5	SA_DQ[35]
36	M_A_DQ<36>	AH5	SA_DQ[36]
37	M_A_DQ<37>	AH6	SA_DQ[37]
38	M_A_DQ<38>	AJ5	SA_DQ[38]
39	M_A_DQ<39>	AJ6	SA_DQ[39]
40	M_A_DQ<40>	AJ8	SA_DQ[40]
41	M_A_DQ<41>	AK8	SA_DQ[41]
42	M_A_DQ<42>	AJ9	SA_DQ[42]
43	M_A_DQ<43>	AK9	SA_DQ[43]
44	M_A_DQ<44>	AH8	SA_DQ[44]
45	M_A_DQ<45>	AH9	SA_DQ[45]
46	M_A_DQ<46>	AL9	SA_DQ[46]
47	M_A_DQ<47>	AL8	SA_DQ[47]
48	M_A_DQ<48>	AP11	SA_DQ[48]
49	M_A_DQ<49>	AN11	SA_DQ[49]
50	M_A_DQ<50>	AL12	SA_DQ[50]
51	M_A_DQ<51>	AM12	SA_DQ[51]
52	M_A_DQ<52>	AM11	SA_DQ[52]
53	M_A_DQ<53>	AL11	SA_DQ[53]
54	M_A_DQ<54>	AP12	SA_DQ[54]
55	M_A_DQ<55>	AN12	SA_DQ[55]
56	M_A_DQ<56>	AJ14	SA_DQ[56]
57	M_A_DQ<57>	AH14	SA_DQ[57]
58	M_A_DQ<58>	AL15	SA_DQ[58]
59	M_A_DQ<59>	AK15	SA_DQ[59]
60	M_A_DQ<60>	AL14	SA_DQ[60]
61	M_A_DQ<61>	AK14	SA_DQ[61]
62	M_A_DQ<62>	AJ15	SA_DQ[62]
63	M_A_DQ<63>	AH15	SA_DQ[63]

42D8	41D8	OUT	M_A_BS0	AE10	SA_BS[0]
42D8	41D8	OUT	M_A_BS1	AF10	SA_BS[1]
42D8	41D8	OUT	M_A_BS2	V6	SA_BS[2]

42C8	41C8	OUT	M_A_CAS#	AE8	SA_CAS#
42C8	41C8	OUT	M_A_RAS#	AD9	SA_RAS#
42C8	41C8	OUT	M_A_WE#	AF9	SA_WE#

DDR SYSTEM MEMORY A

SA_CLK[0]	AB6	M_CLK_DDR0_DP	OUT	41C8
SA_CLK#0[0]	AA6	M_CLK_DDR0_DN	OUT	41C8
SA_CKE[0]	V9	M_CKE0	OUT	41C8
SA_CLK[1]	AA5	M_CLK_DDR1_DP	OUT	41C8
SA_CLK#1[1]	AB5	M_CLK_DDR1_DN	OUT	41C8
SA_CKE[1]	V10	M_CKE1	OUT	41C8
RSVD_TP[1]	AB4	M_CLK_DDR4_DP	OUT	42C8
RSVD_TP[2]	AA4	M_CLK_DDR4_DN	OUT	42C8
RSVD_TP[3]	W9	M_CKE4	OUT	42C8
RSVD_TP[4]	AB3	M_CLK_DDR5_DP	OUT	42C8
RSVD_TP[5]	AA3	M_CLK_DDR5_DN	OUT	42C8
RSVD_TP[6]	W10	M_CKE5	OUT	42C8
SA_CS#0[0]	AK3	M_CS#0	OUT	41D8
SA_CS#1[1]	AL3	M_CS#1	OUT	41C8
RSVD_TP[7]	AG1	M_CS#4	OUT	42D8
RSVD_TP[8]	AH1	M_CS#5	OUT	42C8
SA_ODT[0]	AH3	M_ODT0	OUT	41C8
SA_ODT[1]	AG3	M_ODT1	OUT	41C8
RSVD_TP[9]	AG2	M_ODT4	OUT	42C8
RSVD_TP[10]	AH2	M_ODT5	OUT	42C8
SA_DQS[0]	C4	M_A_DQS0_DN	OUT	41B8 42B8
SA_DQS[1]	G6	M_A_DQS1_DN	OUT	41B8 42B8
SA_DQS[2]	J3	M_A_DQS2_DN	OUT	41B8 42B8
SA_DQS[3]	M6	M_A_DQS3_DN	OUT	41B8 42B8
SA_DQS[4]	AL6	M_A_DQS4_DN	OUT	41B8 42B8
SA_DQS[5]	AM8	M_A_DQS5_DN	OUT	41B8 42B8
SA_DQS[6]	AR12M	M_A_DQS6_DN	OUT	41B8 42B8
SA_DQS[7]	AM15M	M_A_DQS7_DN	OUT	41B8 42B8
SA_DQS[0]	D4	M_A_DQS0_DP	OUT	41B8 42B8
SA_DQS[1]	F6	M_A_DQS1_DP	OUT	41B8 42B8
SA_DQS[2]	K3	M_A_DQS2_DP	OUT	41B8 42B8
SA_DQS[3]	N6	M_A_DQS3_DP	OUT	41B8 42B8
SA_DQS[4]	AL5	M_A_DQS4_DP	OUT	41B8 42B8
SA_DQS[5]	AM9	M_A_DQS5_DP	OUT	41B8 42B8
SA_DQS[6]	AR11M	M_A_DQS6_DP	OUT	41B8 42B8
SA_DQS[7]	AM14M	M_A_DQS7_DP	OUT	41B8 42B8
SA_MA[0]	AD10	M_A_A<0>	OUT	41D8 42D8
SA_MA[1]	W1	M_A_A<1>	OUT	41D8 42D8
SA_MA[2]	W2	M_A_A<2>	OUT	41D8 42D8
SA_MA[3]	W7	M_A_A<3>	OUT	41D8 42D8
SA_MA[4]	V3	M_A_A<4>	OUT	41D8 42D8
SA_MA[5]	V2	M_A_A<5>	OUT	41D8 42D8
SA_MA[6]	W3	M_A_A<6>	OUT	41D8 42D8
SA_MA[7]	W6	M_A_A<7>	OUT	41D8 42D8
SA_MA[8]	V1	M_A_A<8>	OUT	41D8 42D8
SA_MA[9]	W5	M_A_A<9>	OUT	41D8 42D8
SA_MA[10]	AD8	M_A_A<10>	OUT	41D8 42D8
SA_MA[11]	V4	M_A_A<11>	OUT	41D8 42D8
SA_MA[12]	W4	M_A_A<12>	OUT	41D8 42D8
SA_MA[13]	AF8	M_A_A<13>	OUT	41D8 42D8
SA_MA[14]	V5	M_A_A<14>	OUT	41D8 42D8
SA_MA[15]	V7	M_A_A<15>	OUT	41D8 42D8

M_A_A<15..0>

44D8	43D8	OUT	M_B_BS0	AA9	SB_BS[0]
44D8	43D8	OUT	M_B_BS1	AA7	SB_BS[1]
44C8	43C8	OUT	M_B_BS2	R6	SB_BS[2]

44C8	43C8	OUT	M_B_CAS#	AA10	SB_CAS#
44C8	43C8	OUT	M_B_RAS#	AB8	SB_RAS#
44C8	43C8	OUT	M_B_WE#	AB9	SB_WE#

44D5 43D5 BI M_B_DQ<63..0>

0	M_B_DQ<0>	C9	SB_DQ[0]
1	M_B_DQ<1>	A7	SB_DQ[1]
2	M_B_DQ<2>	D10	SB_DQ[2]
3	M_B_DQ<3>	C8	SB_DQ[3]
4	M_B_DQ<4>	A9	SB_DQ[4]
5	M_B_DQ<5>	A8	SB_DQ[5]
6	M_B_DQ<6>	D9	SB_DQ[6]
7	M_B_DQ<7>	D8	SB_DQ[7]
8	M_B_DQ<8>	G4	SB_DQ[8]
9	M_B_DQ<9>	F4	SB_DQ[9]
10	M_B_DQ<10>	F1	SB_DQ[10]
11	M_B_DQ<11>	G1	SB_DQ[11]
12	M_B_DQ<12>	G5	SB_DQ[12]
13	M_B_DQ<13>	F5	SB_DQ[13]
14	M_B_DQ<14>	F2	SB_DQ[14]
15	M_B_DQ<15>	G2	SB_DQ[15]
16	M_B_DQ<16>	J7	SB_DQ[16]
17	M_B_DQ<17>	J8	SB_DQ[17]
18	M_B_DQ<18>	K10	SB_DQ[18]
19	M_B_DQ<19>	K9	SB_DQ[19]
20	M_B_DQ<20>	J9	SB_DQ[20]
21	M_B_DQ<21>	J10	SB_DQ[21]
22	M_B_DQ<22>	K8	SB_DQ[22]
23	M_B_DQ<23>	K7	SB_DQ[23]
24	M_B_DQ<24>	M5	SB_DQ[24]
25	M_B_DQ<25>	N4	SB_DQ[25]
26	M_B_DQ<26>	N2	SB_DQ[26]
27	M_B_DQ<27>	N1	SB_DQ[27]
28	M_B_DQ<28>	M4	SB_DQ[28]
29	M_B_DQ<29>	N5	SB_DQ[29]
30	M_B_DQ<30>	M2	SB_DQ[30]
31	M_B_DQ<31>	M1	SB_DQ[31]
32	M_B_DQ<32>	AM5	SB_DQ[32]
33	M_B_DQ<33>	AM6	SB_DQ[33]
34	M_B_DQ<34>	AR3	SB_DQ[34]
35	M_B_DQ<35>	AP3	SB_DQ[35]
36	M_B_DQ<36>	AN3	SB_DQ[36]
37	M_B_DQ<37>	AN2	SB_DQ[37]
38	M_B_DQ<38>	AN1	SB_DQ[38]
39	M_B_DQ<39>	AP2	SB_DQ[39]
40	M_B_DQ<40>	AP5	SB_DQ[40]
41	M_B_DQ<41>	AN9	SB_DQ[41]
42	M_B_DQ<42>	AT5	SB_DQ[42]
43	M_B_DQ<43>	AT6	SB_DQ[43]
44	M_B_DQ<44>	AP6	SB_DQ[44]
45	M_B_DQ<45>	AN8	SB_DQ[45]
46	M_B_DQ<46>	AR6	SB_DQ[46]
47	M_B_DQ<47>	AR5	SB_DQ[47]
48	M_B_DQ<48>	AR9	SB_DQ[48]
49	M_B_DQ<49>	AN11	SB_DQ[49]
50	M_B_DQ<50>	AT8	SB_DQ[50]
51	M_B_DQ<51>	AT9	SB_DQ[51]
52	M_B_DQ<52>	AN11	SB_DQ[52]
53	M_B_DQ<53>	AR8	SB_DQ[53]
54	M_B_DQ<54>	AN12	SB_DQ[54]
55	M_B_DQ<55>	AN12	SB_DQ[55]
56	M_B_DQ<56>	AN11	SB_DQ[56]
57	M_B_DQ<57>	AN14	SB_DQ[57]
58	M_B_DQ<58>	AN14	SB_DQ[58]
59	M_B_DQ<59>	AN14	SB_DQ[59]
60	M_B_DQ<60>	AN12	SB_DQ[60]
61	M_B_DQ<61>	AN15	SB_DQ[61]
62	M_B_DQ<62>	AN15	SB_DQ[62]
63	M_B_DQ<63>	AN15	SB_DQ[63]

CN4500

DDR SYSTEM MEMORY B

SB_CLK[0]	AE2	M_CLK_DDR2_DP	OUT	43C8
SB_CLK#0[0]	AD2	M_CLK_DDR2_DN	OUT	43C8
SB_CKE[0]	R9	M_CKE2	OUT	43C8
SB_CLK[1]	AE1	M_CLK_DDR3_DP	OUT	43C8
SB_CLK#1[1]	AD1	M_CLK_DDR3_DN	OUT	43C8
SB_CKE[1]	R10	M_CKE3	OUT	43C8
RSVD_TP[11]	AB2	M_CLK_DDR6_DP	OUT	44C8
RSVD_TP[12]	AA2	M_CLK_DDR6_DN	OUT	44C8
RSVD_TP[13]	T9	M_CKE6	OUT	44C8
RSVD_TP[14]	AA1	M_CLK_DDR7_DP	OUT	44C8
RSVD_TP[15]	AB1	M_CLK_DDR7_DN	OUT	44C8
RSVD_TP[16]	T10	M_CKE7	OUT	44C8
SB_CS#0[0]	AD3	M_CS#2	OUT	43C8
SB_CS#1[1]	AE3	M_CS#3	OUT	43C8
RSVD_TP[17]	AD6	M_CS#6	OUT	44C8
RSVD_TP[18]	AE6	M_CS#7	OUT	44C8
SB_ODT[0]	AE4	M_ODT2	OUT	43C8
SB_ODT[1]	AD4	M_ODT3	OUT	43C8
RSVD_TP[19]	AD5	M_ODT6	OUT	44C8
RSVD_TP[20]	AE5	M_ODT7	OUT	44C8
SB_DQS[0]	D7	M_B_DQS0_DN	OUT	43B8 44B8
SB_DQS[1]	F3	M_B_DQS1_DN	OUT	43B8 44B8
SB_DQS[2]	K6	M_B_DQS2_DN	OUT	43B8 44B8
SB_DQS[3]	N3	M_B_DQS3_DN	OUT	43B8 44B8
SB_DQS[4]	AN5	M_B_DQS4_DN	OUT	43B8 44B8
SB_DQS[5]	AP9	M_B_DQS5_DN	OUT	43B8 44B8
SB_DQS[6]	AK12	M_B_DQS6_DN	OUT	43B8 44B8
SB_DQS[7]	AP15	M_B_DQS7_DN	OUT	43B8 44B8
SB_DQS[0]	C7	M_B_DQS0_DP	OUT	43B8 44B8
SB_DQS[1]	G3	M_B_DQS1_DP	OUT	43B8 44B8
SB_DQS[2]	J6	M_B_DQS2_DP	OUT	43B8 44B8
SB_DQS[3]	M3	M_B_DQS3_DP	OUT	43B8 44B8
SB_DQS[4]	AN6	M_B_DQS4_DP	OUT	43B8 44B8
SB_DQS[5]	AP8	M_B_DQS5_DP	OUT	43B8 44B8
SB_DQS[6]	AK11	M_B_DQS6_DP	OUT	43B8 44B8
SB_DQS[7]	AP14	M_B_DQS7_DP	OUT	43B8 44B8
SB_MA[0]	AA8	M_B_A<0>	OUT	43B8 44B8
SB_MA[1]	T7	M_B_A<1>	OUT	43B8 44B8
SB_MA[2]	R7	M_B_A<2>	OUT	43B8 44B8
SB_MA[3]	T6	M_B_A<3>	OUT	43B8 44B8
SB_MA[4]	T2	M_B_A<4>	OUT	43B8 44B8
SB_MA[5]	T4	M_B_A<5>	OUT	43B8 44B8
SB_MA[6]	T3	M_B_A<6>	OUT	43B8 44B8
SB_MA[7]	R2	M_B_A<7>	OUT	43B8 44B8
SB_MA[8]	T5	M_B_A<8>	OUT	43B8 44B8
SB_MA[9]	R3	M_B_A<9>	OUT	43B8 44B8
SB_MA[10]	AB7	M_B_A<10>	OUT	43B8 44B8
SB_MA[11]	R1	M_B_A<11>	OUT	43B8 44B8
SB_MA[12]	T1	M_B_A<12>	OUT	43B8 44B8
SB_MA[13]	AB10	M_B_A<13>	OUT	43B8 44B8
SB_MA[14]	R5	M_B_A<14>	OUT	43B8 44B8
SB_MA[15]	R4	M_B_A<15>	OUT	43B8 44B8

M_B_A<15..0>

FOX_PZ98927_3641_41F_HURONRIVER_989P_CHIEFRIVER

INVENTEC

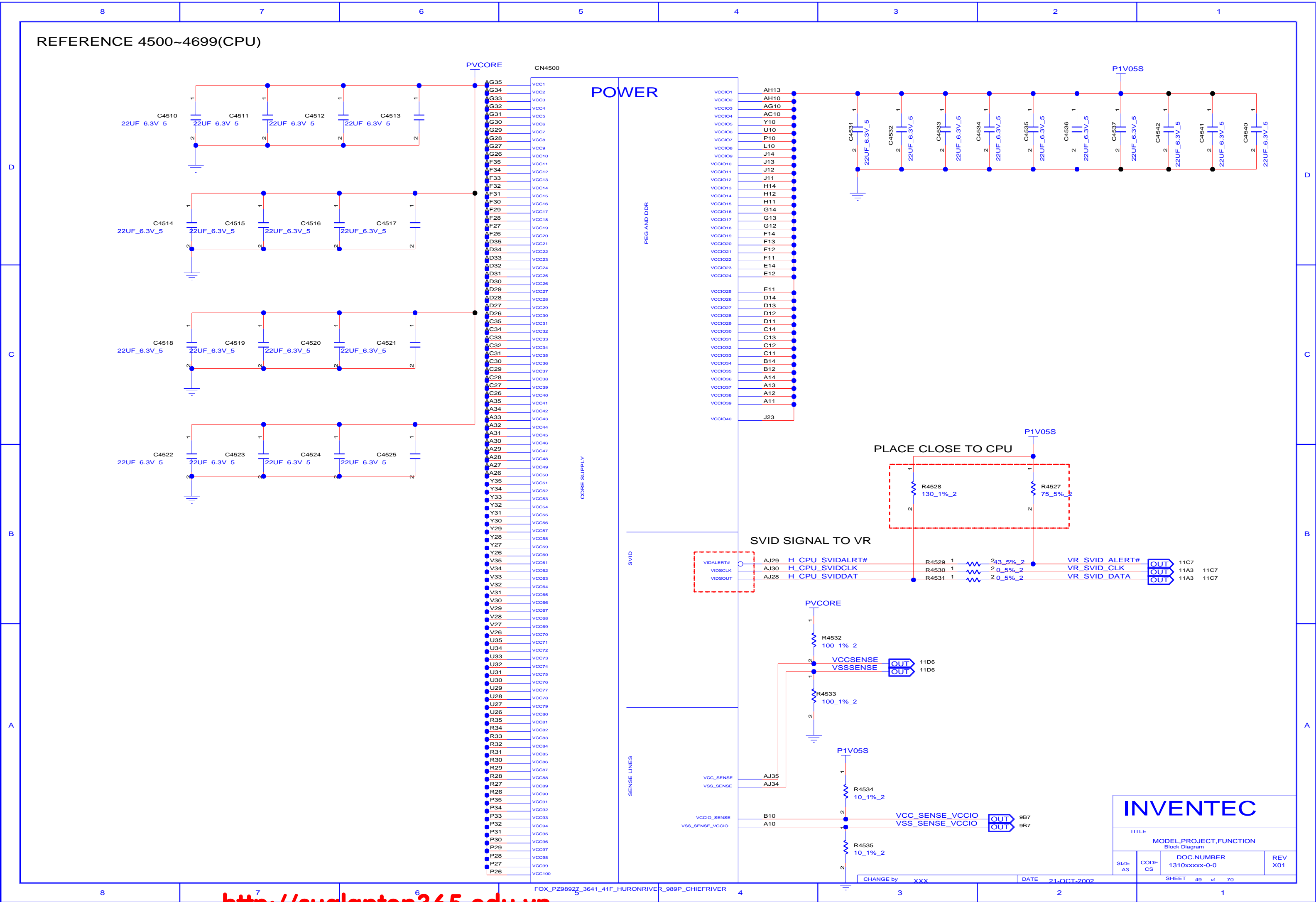
TITLE

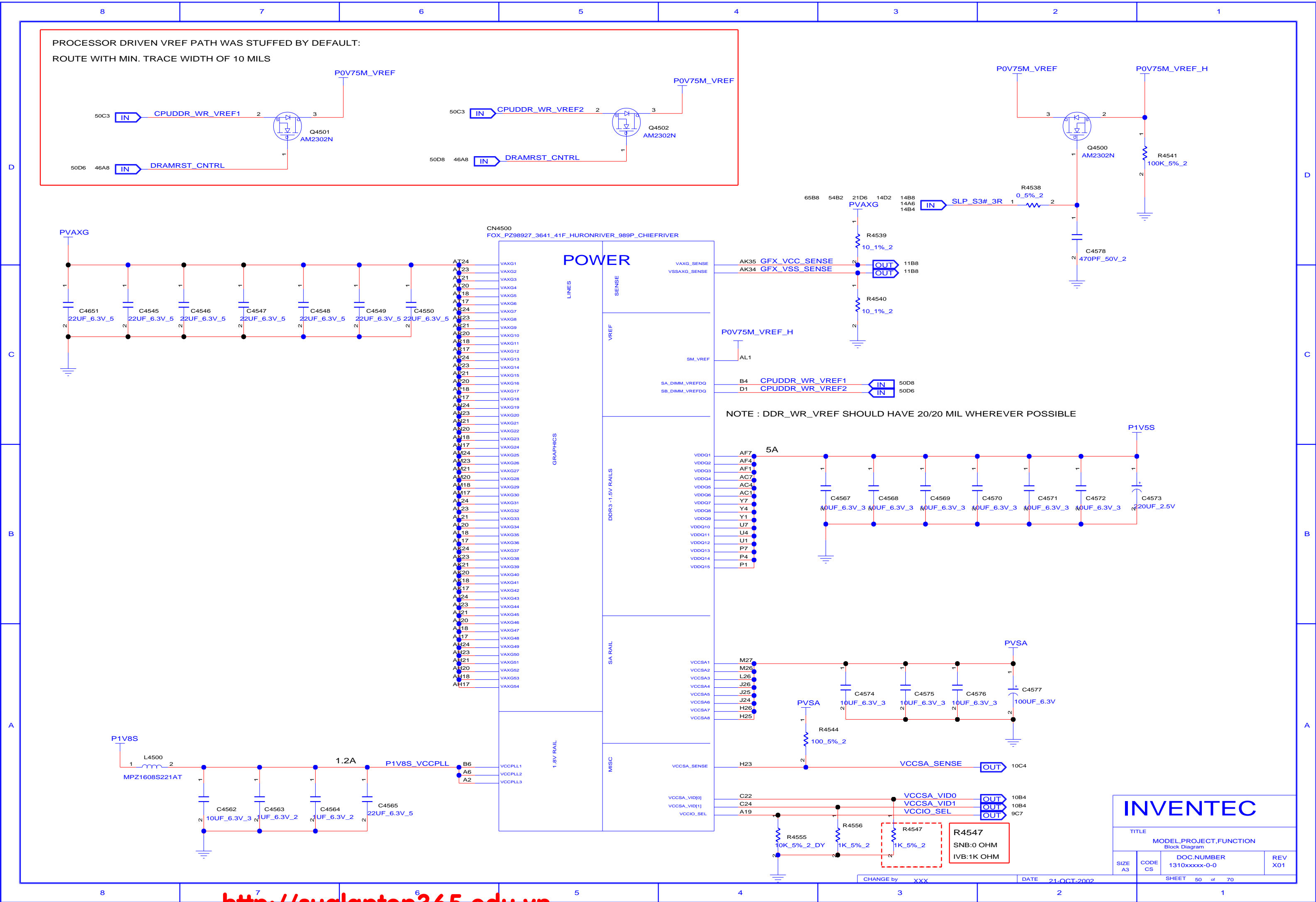
MODEL,PROJECT,FUNCTION

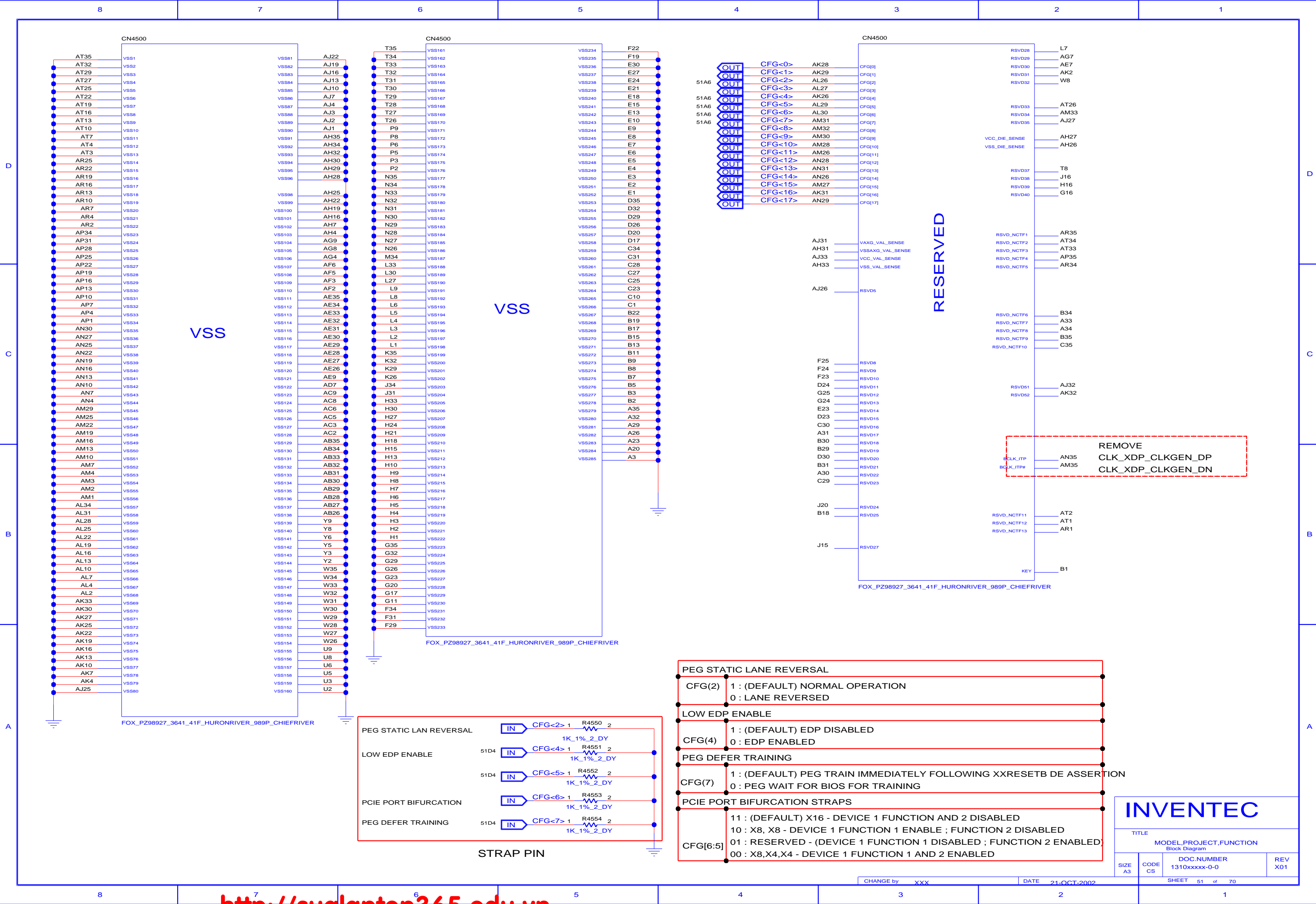
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

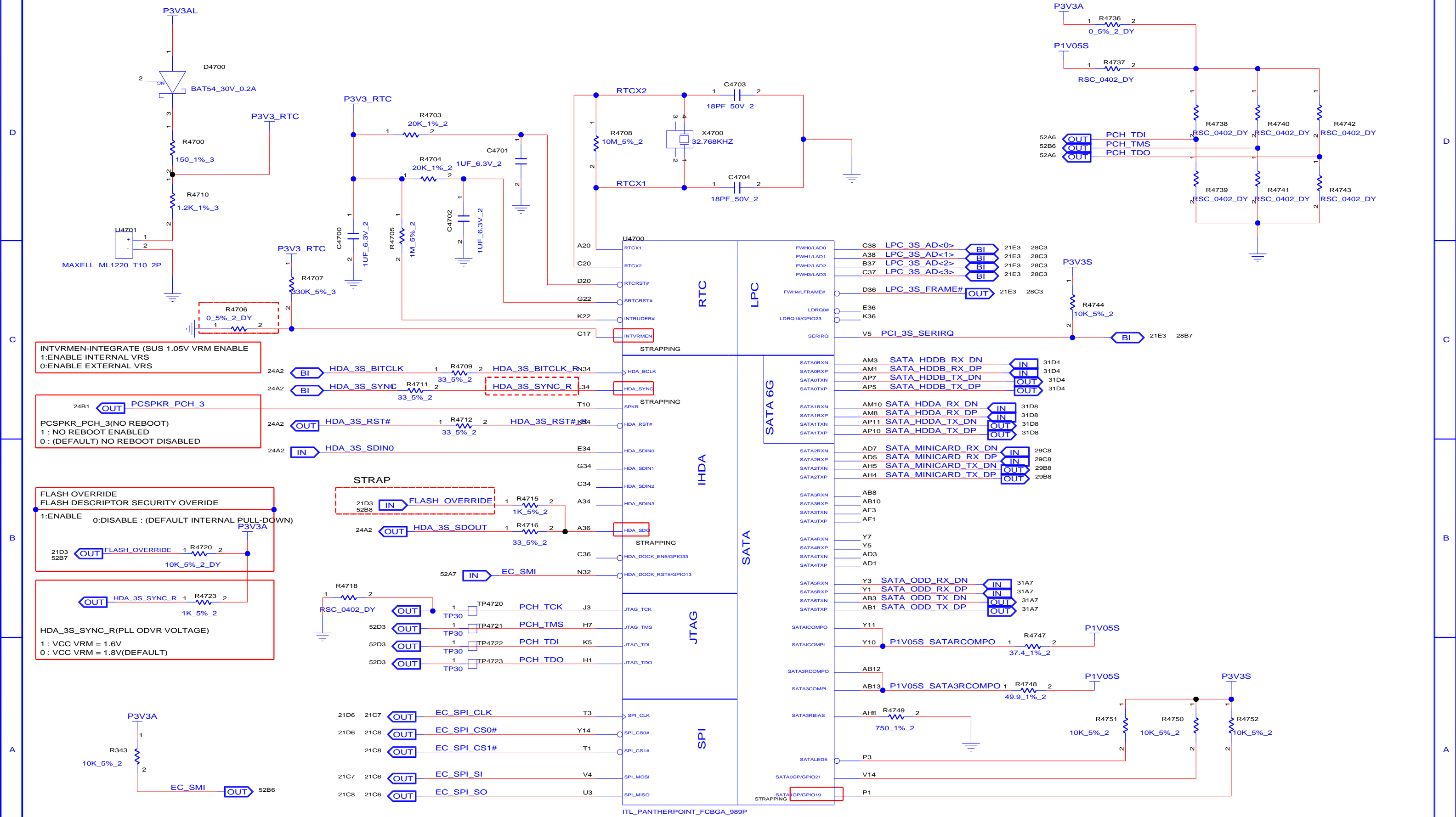
CHANGE by





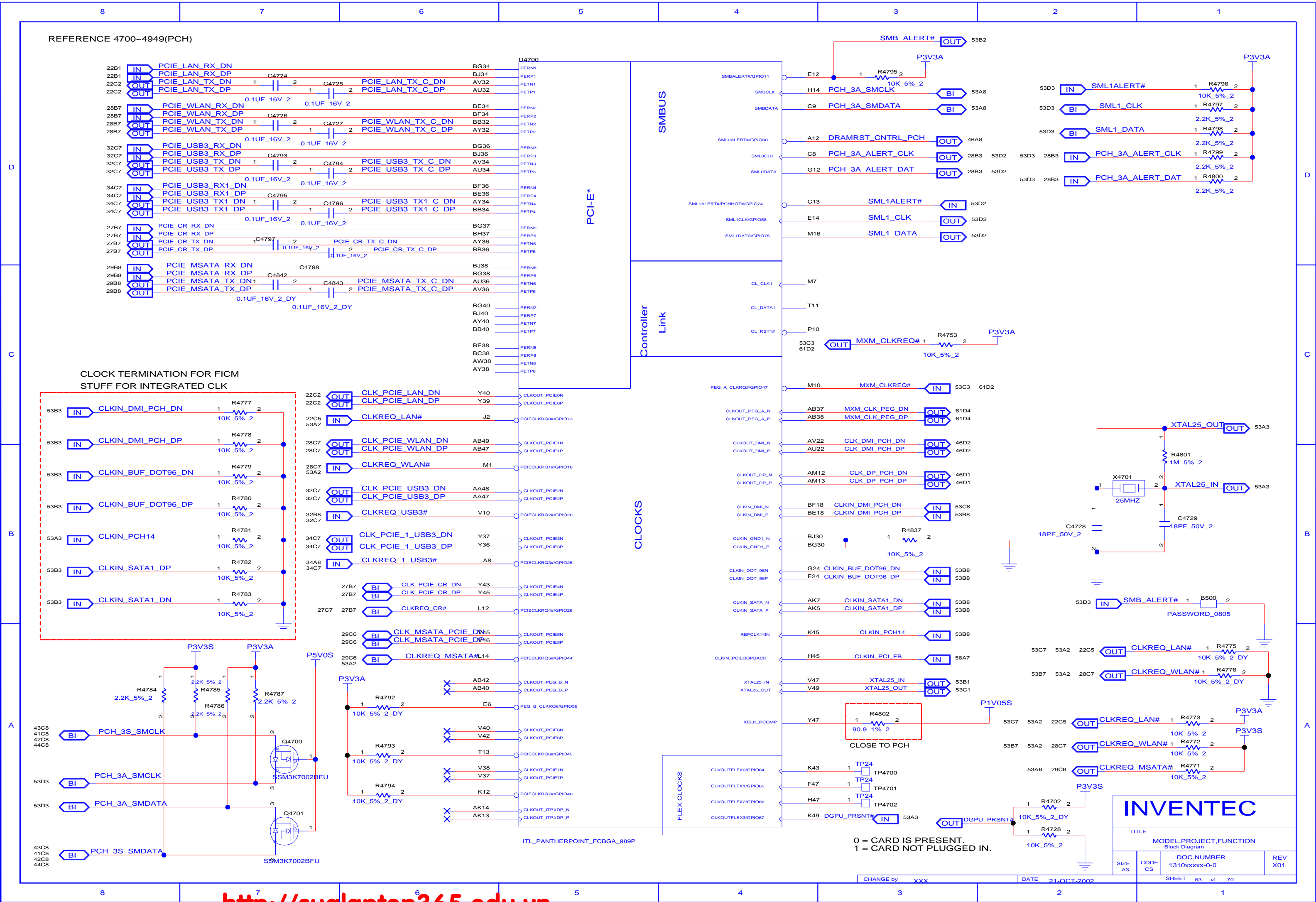


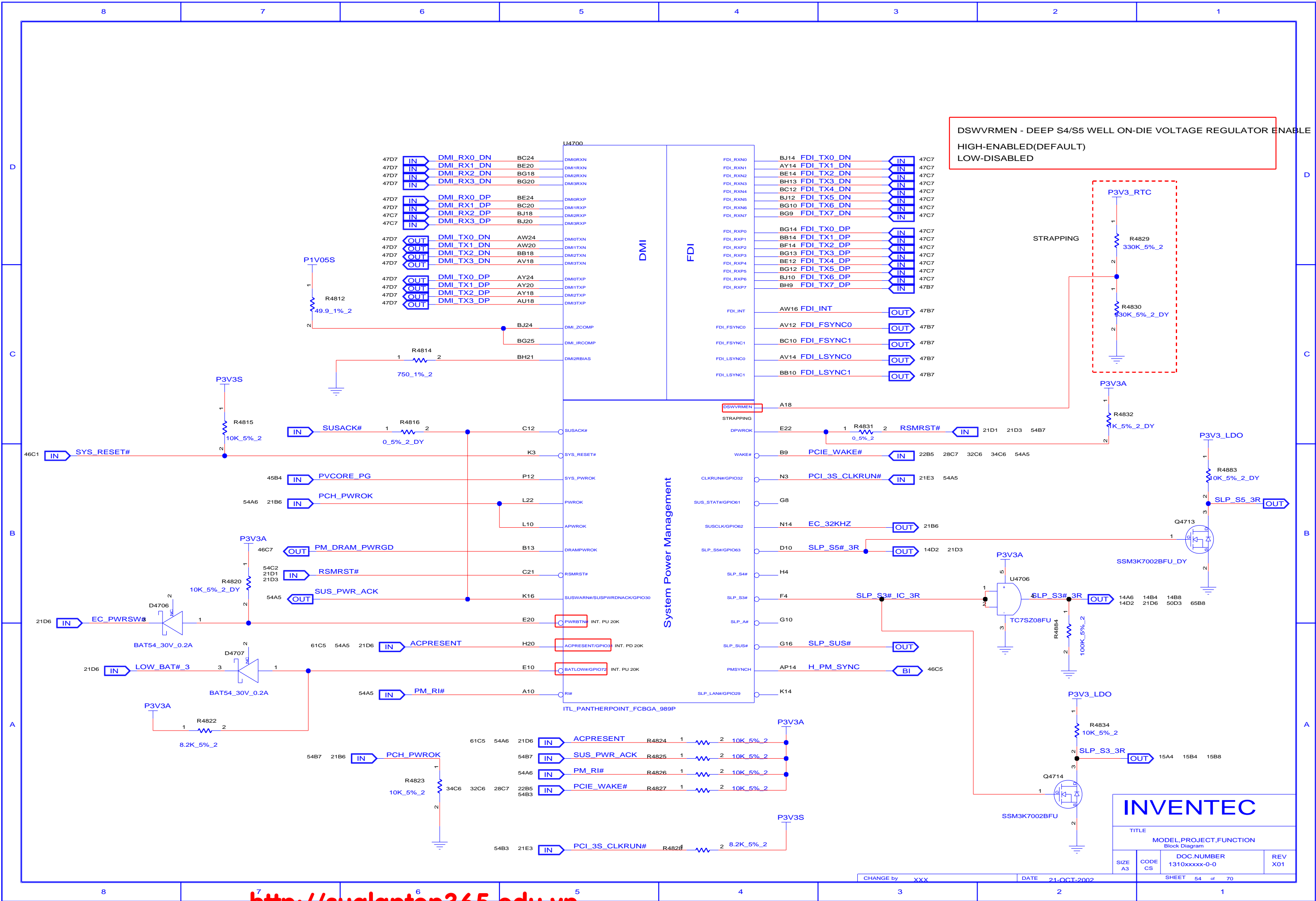
REFERENCE 4700~4949(PCH)

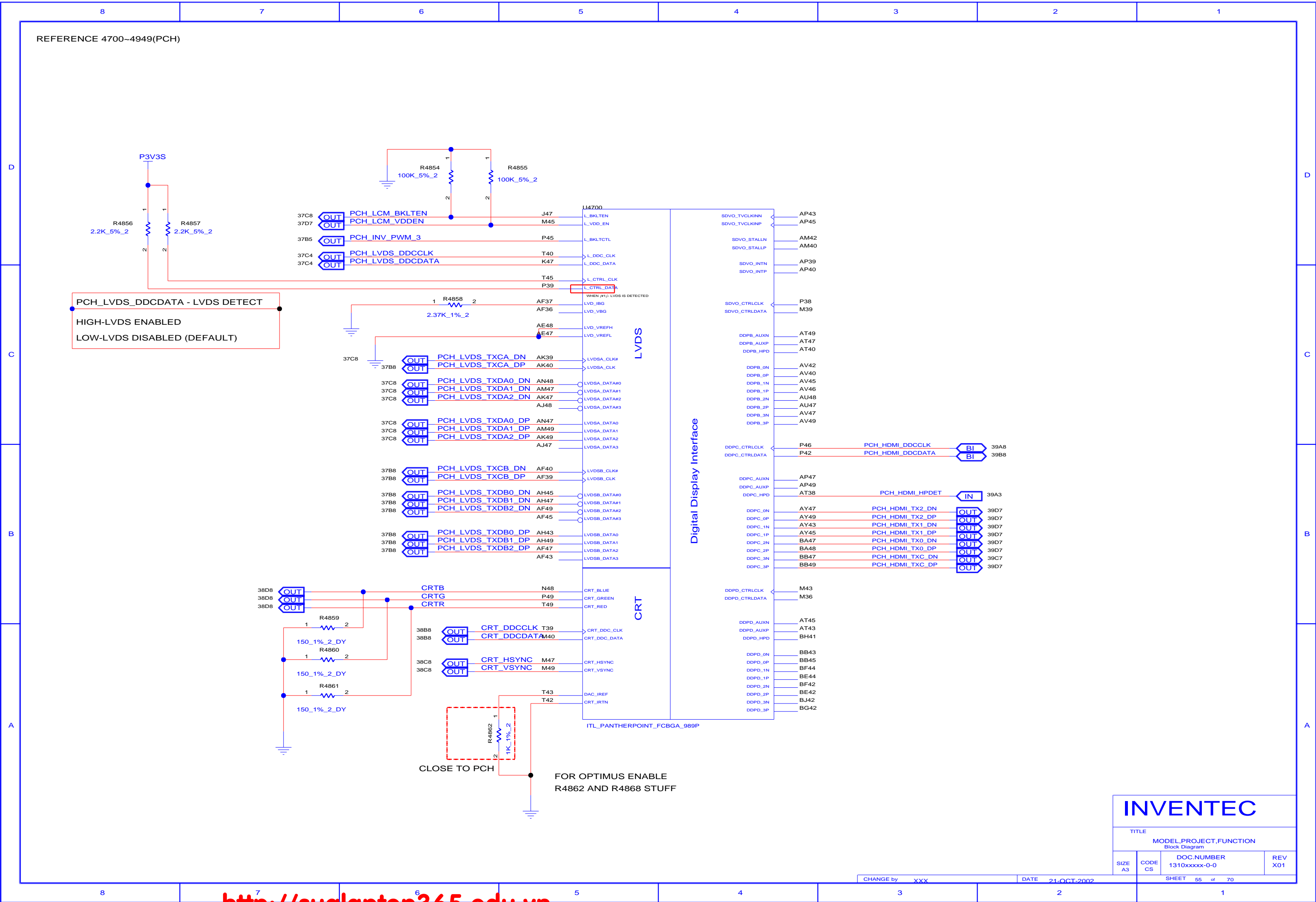


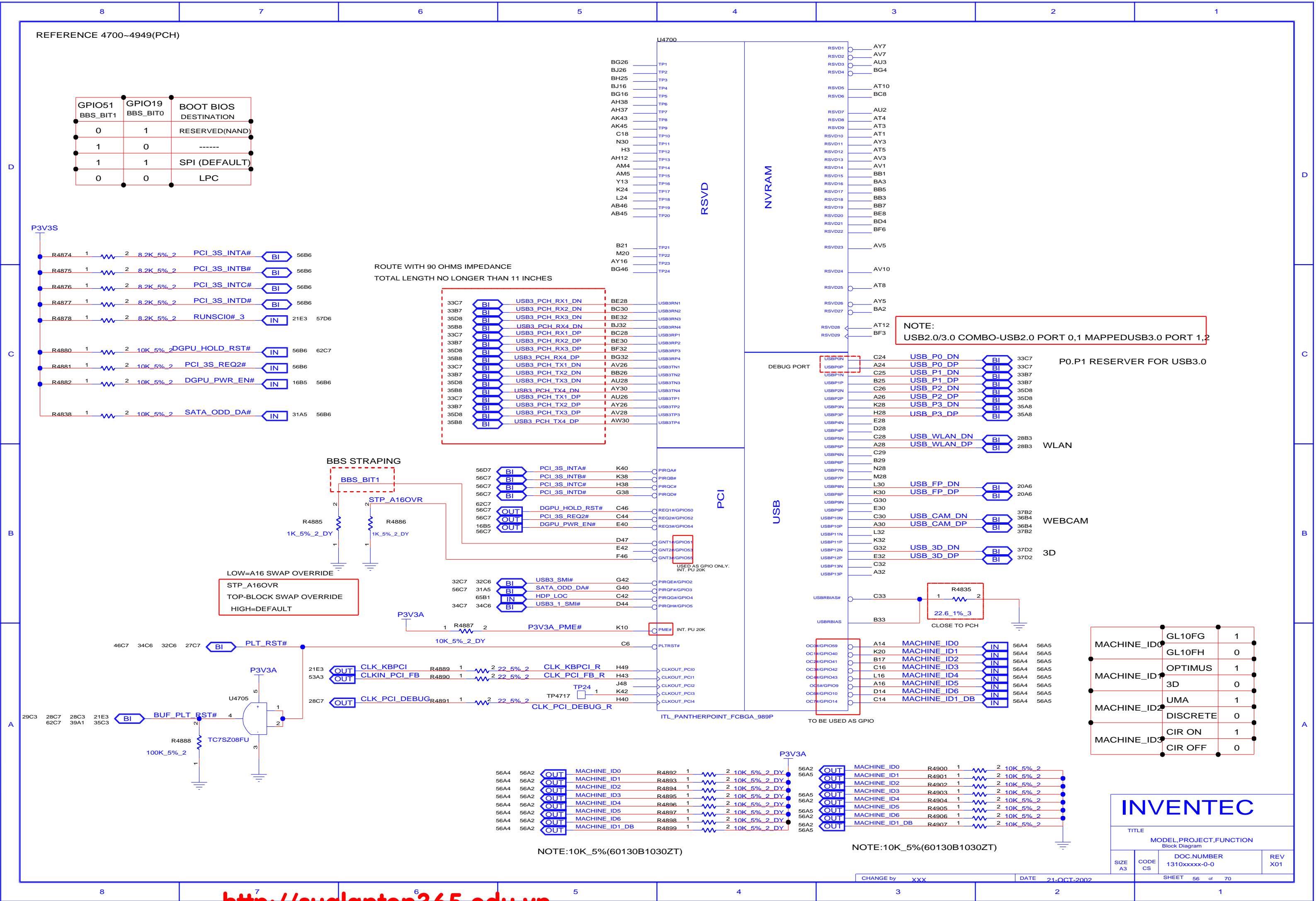
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 52 of 70



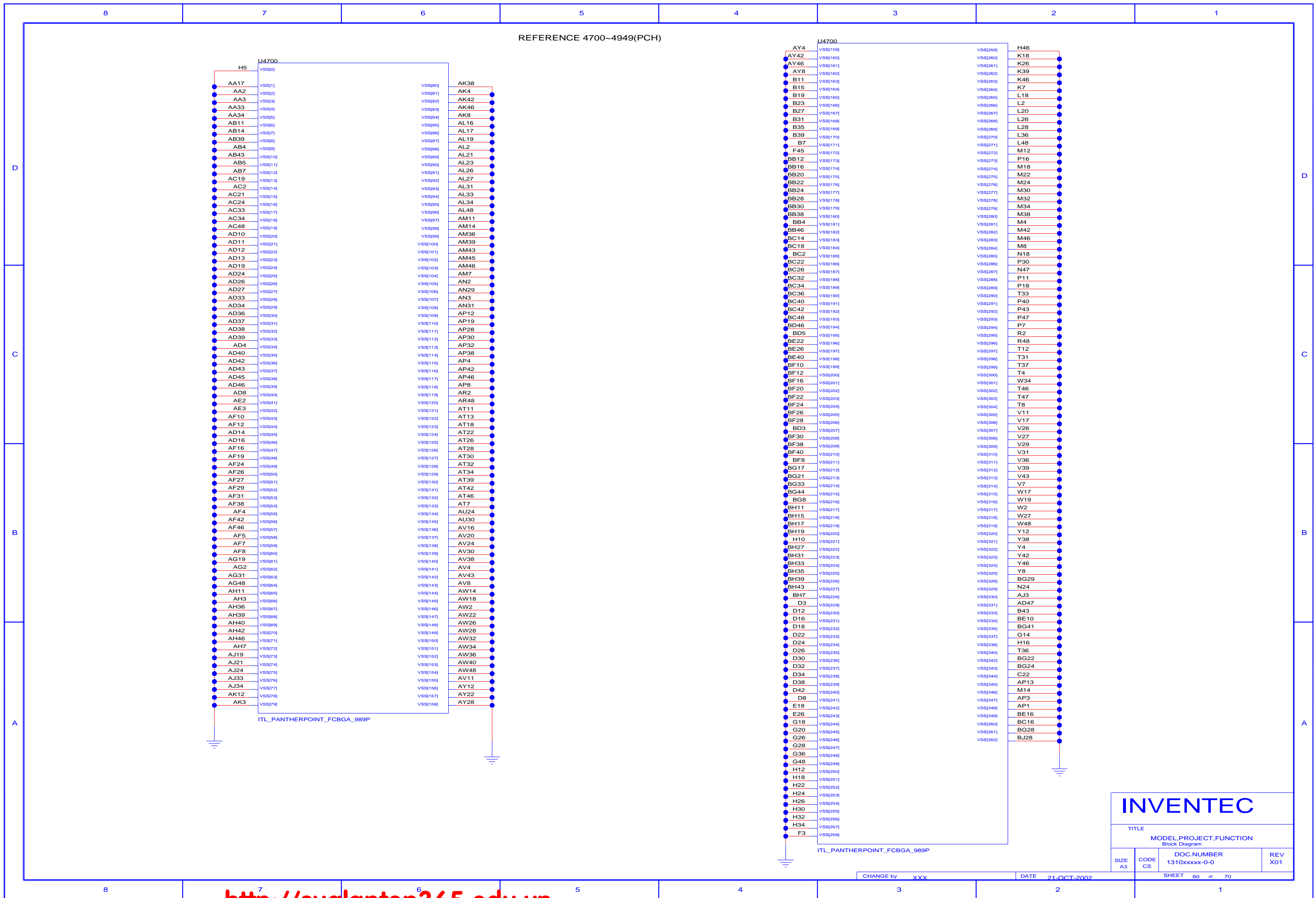


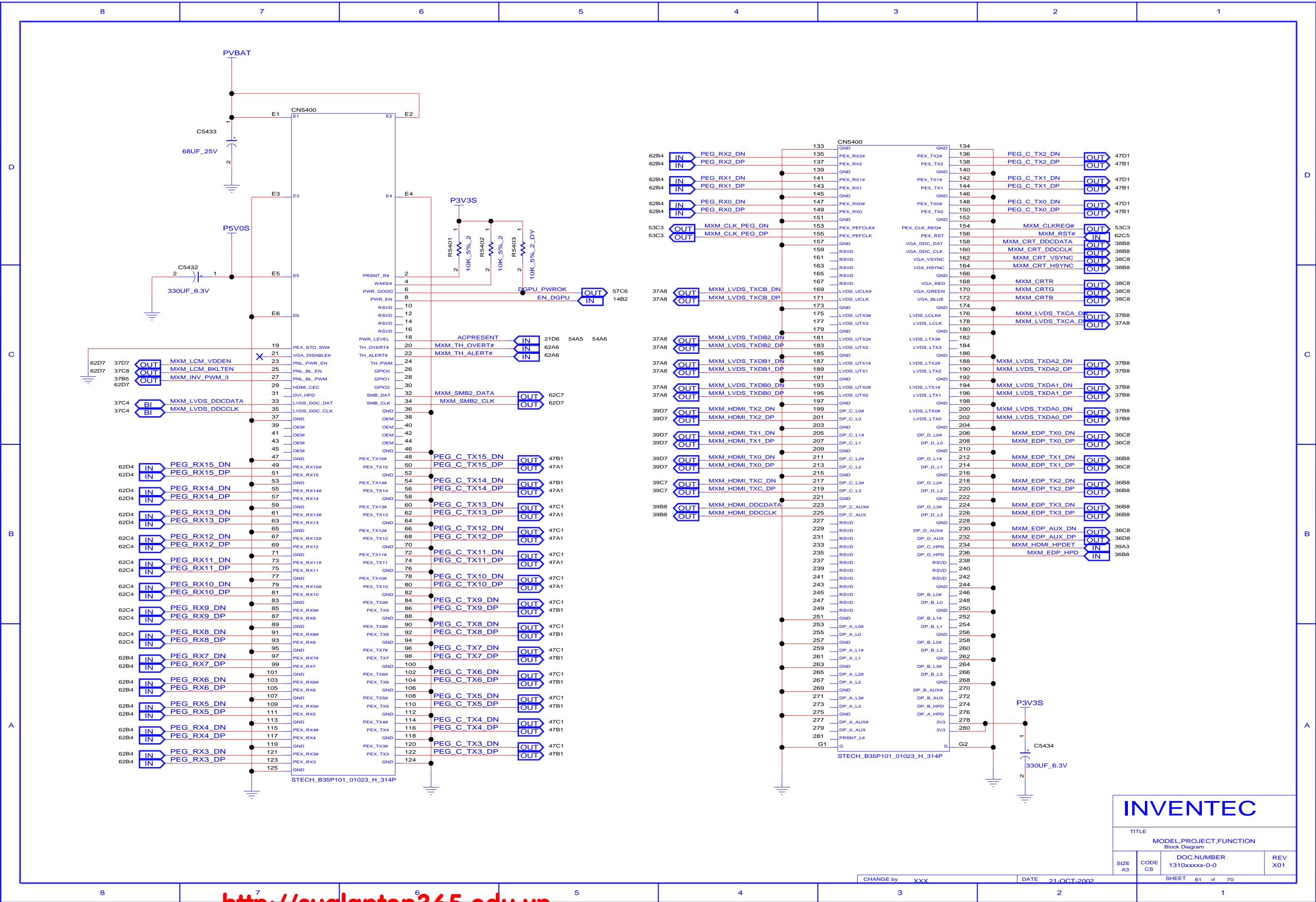


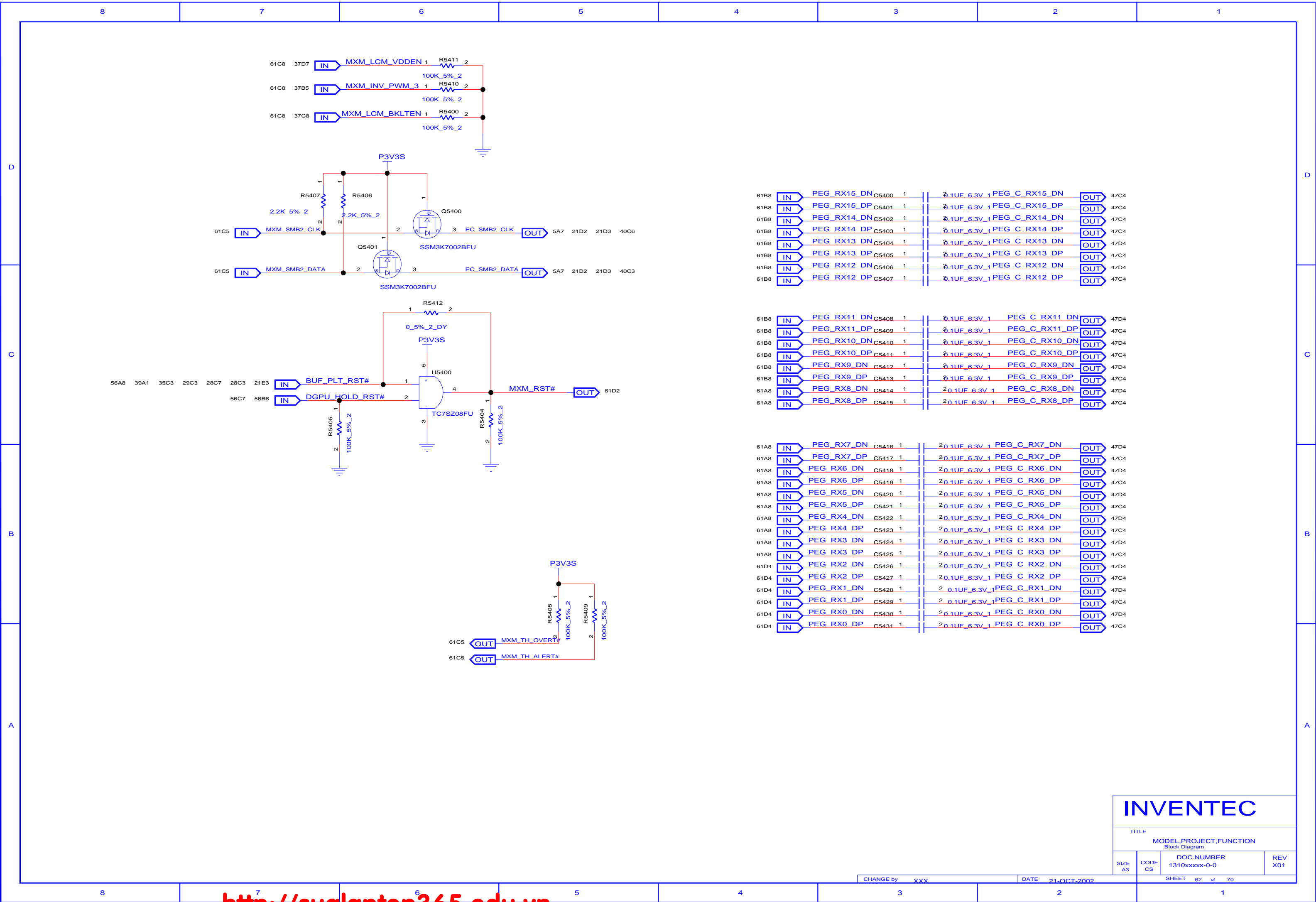


[illegible]



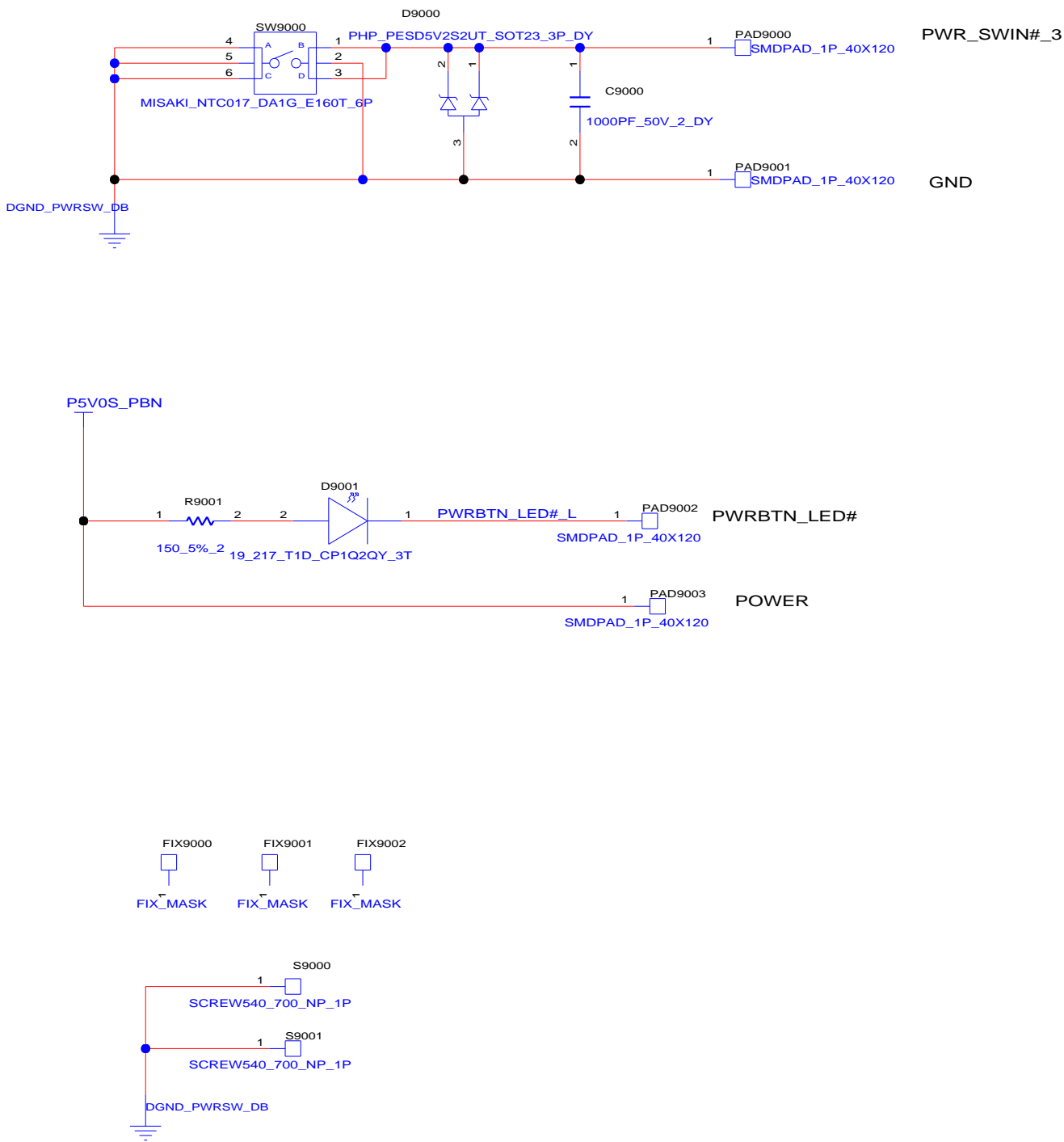






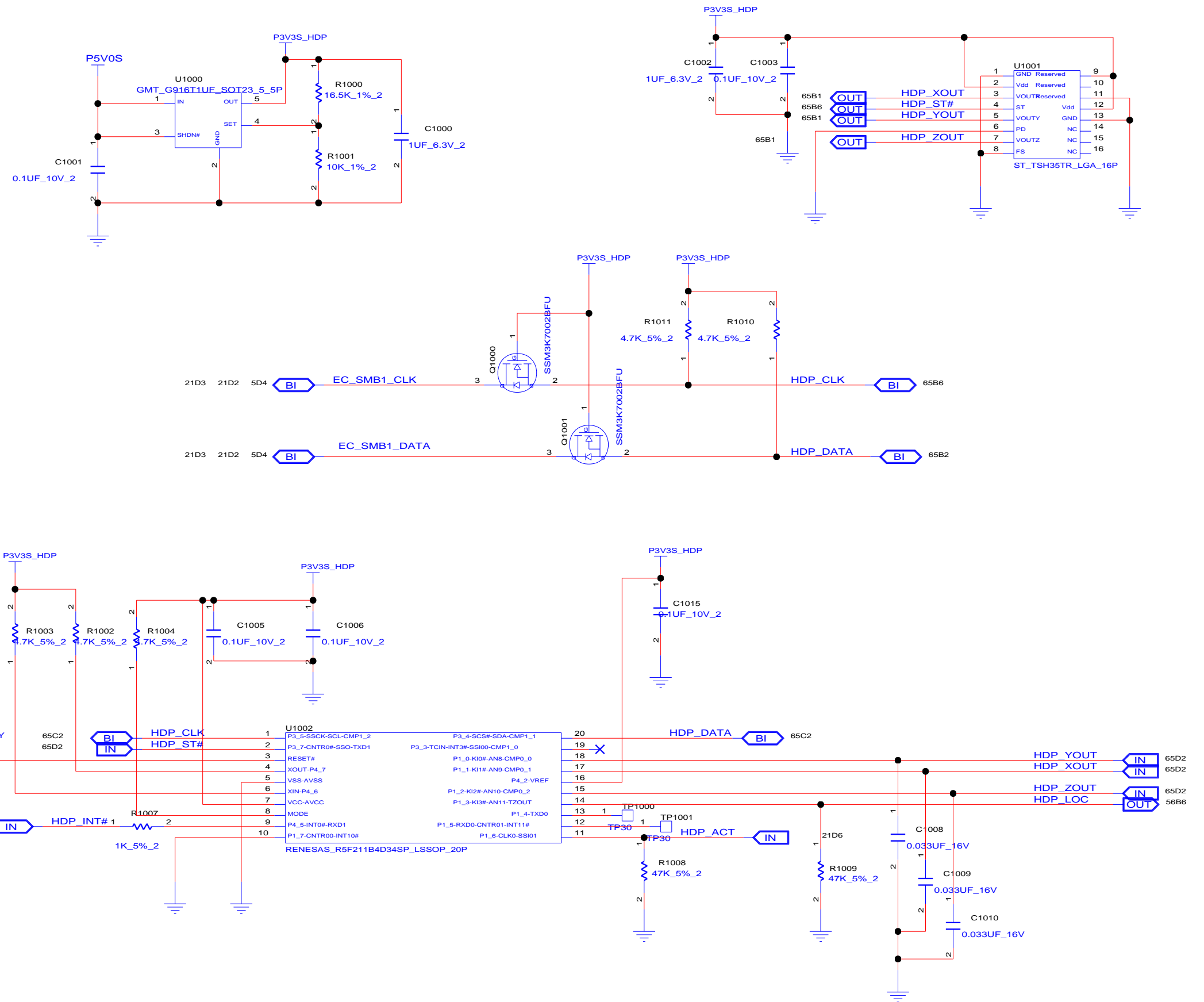
REFERENCE 9000~9999(SMALL BOARD)

POWER BUTTON



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 63 of 70

REFERENCE 1000~1099(3D SENSOR)



INVENTEC

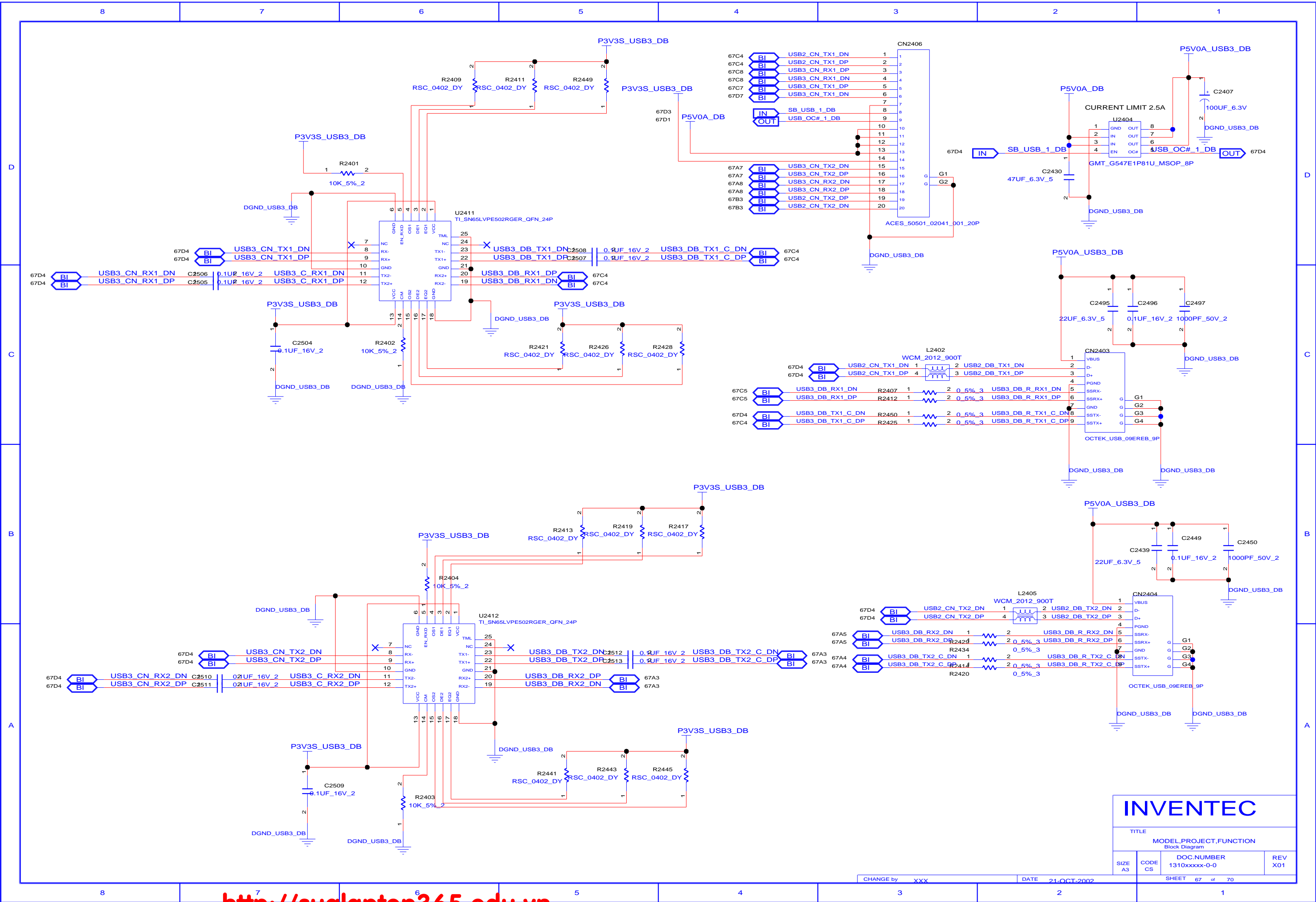
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 65 of 70

<http://sualaptop365.edu.vn>

8	7	6	5	4	3	2	1																
REFERENCE 390~399																							
D							D																
C							C																
B							B																
A							A																
					<table><tr><td colspan="4">INVENTEC</td></tr><tr><td colspan="4">TITLE MODEL,PROJECT,FUNCTION Block Diagram</td></tr><tr><td>SIZE A3</td><td>CODE CS</td><td>DOC.NUMBER 1310xxxxx-0-0</td><td>REV X01</td></tr><tr><td colspan="2">CHANGE by XXX</td><td>DATE 21-OCT-2002</td><td>SHEET 66 of 70</td></tr></table>			INVENTEC				TITLE MODEL,PROJECT,FUNCTION Block Diagram				SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01	CHANGE by XXX		DATE 21-OCT-2002	SHEET 66 of 70
INVENTEC																							
TITLE MODEL,PROJECT,FUNCTION Block Diagram																							
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01																				
CHANGE by XXX		DATE 21-OCT-2002	SHEET 66 of 70																				
8	7	6	5	4	3	2	1																



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 67 of 70

<http://sualaptop365.edu.vn>

8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

INVENTEC

TITLEMODEL,PROJECT,FUNCTIONBlock Diagram

SIZEA3

CODECS

DOC.NUMBER1310xxxxx-0-0

REVX01

CHANGE byXXXDATE21-OCT-2002SHEET68 of 70

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE A6	CODE C6	DOC.NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

SHEET 69 of 70

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



A

8	7	6	5	4	3	2	1
http://cud.anton365.edu.vn							